

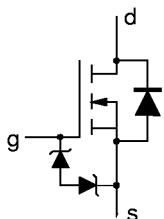
TrenchMOS™ transistor Logic level FET

PHP50N06LT, PHB50N06LT, PHD50N06LT

FEATURES

- 'Trench' technology
- Very low on-state resistance
- Fast switching
- Stable off-state characteristics
- High thermal cycling performance
- Low thermal resistance

SYMBOL



QUICK REFERENCE DATA

$V_{DSS} = 55 \text{ V}$

$I_D = 50 \text{ A}$

$R_{DS(ON)} \leq 24 \text{ m}\Omega (\text{V}_{GS} = 5 \text{ V})$

$R_{DS(ON)} \leq 22 \text{ m}\Omega (\text{V}_{GS} = 10 \text{ V})$

GENERAL DESCRIPTION

N-channel enhancement mode, logic level, field-effect power transistor in a plastic envelope using 'trench' technology. The device has very low on-state resistance. It is intended for use in dc to dc converters and general purpose switching applications.

The PHP50N06LT is supplied in the SOT78 (TO220AB) conventional leaded package.

The PHB50N06LT is supplied in the SOT404 surface mounting package.

The PHD50N06LT is supplied in the SOT428 surface mounting package.

PINNING

SOT78 (TO220AB)

SOT404

SOT428

PIN	DESCRIPTION	SOT78 (TO220AB)	SOT404	SOT428
1	gate			
2	drain ¹			
3	source			
tab	drain			

LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DSS}	Drain-source voltage	$T_j = 25^\circ\text{C}$ to 175°C	-	55	V
V_{DGR}	Drain-gate voltage	$T_j = 25^\circ\text{C}$ to 175°C ; $R_{GS} = 20 \text{ k}\Omega$	-	55	V
V_{GS}	Gate-source voltage		-	± 13	V
I_D	Continuous drain current	$T_{mb} = 25^\circ\text{C}$	-	50	A
		$T_{mb} = 100^\circ\text{C}$	-	35	A
I_{DM}	Pulsed drain current	$T_{mb} = 25^\circ\text{C}$	-	200	A
P_D	Total power dissipation	$T_{mb} = 25^\circ\text{C}$	-	125	W
T_j, T_{stg}	Operating junction and storage temperature		-55	175	$^\circ\text{C}$

¹ It is not possible to make connection to pin 2 of the SOT428 or SOT404 packages.

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THERMAL RESISTANCES

SYMBOL	PARAMETER	CONDITIONS	TYP.	MAX.	UNIT
$R_{th\ j-mb}$	Thermal resistance junction to mounting base		-	1.2	K/W
$R_{th\ j-a}$	Thermal resistance junction to ambient	SOT78 package, in free air SOT404 and SOT428 package, pcb mounted, minimum footprint	60 50	- -	K/W K/W

ESD LIMITING VALUE

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_C	Electrostatic discharge capacitor voltage, all pins	Human body model (100 pF, 1.5 k Ω)	-	2	kV

ELECTRICAL CHARACTERISTICS

T_i = 25°C unless otherwise specified

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	$V_{GS} = 0 \text{ V}; I_D = 0.25 \text{ mA}$	55	-	-	V
$V_{(BR)GSS}$	Gate-source breakdown voltage	$I_G = \pm 1 \text{ mA}$	50	-	-	V
$V_{GS(TO)}$	Gate threshold voltage	$V_{DS} = V_{GS}; I_D = 1 \text{ mA}$	10	-	-	V
$R_{DS(ON)}$	Drain-source on-state resistance	$V_{GS} = 5 \text{ V}; I_D = 12.5 \text{ A}$ $V_{GS} = 10 \text{ V}; I_D = 12.5 \text{ A}$	1.0 0.5 $T_j = -55^\circ\text{C}$	1.5 - $T_j = 175^\circ\text{C}$	2.0 - 2.3	V V V
g_{fs} I_{GSS}	Forward transconductance Gate source leakage current	$V_{DS} = 25 \text{ V}; I_D = 25 \text{ A}$ $V_{GS} = \pm 5 \text{ V}; V_{DS} = 0 \text{ V}$	$T_j = 175^\circ\text{C}$	19 17 - $T_j = 175^\circ\text{C}$	24 22 50 - 0.02 1 20	$\text{m}\Omega$ $\text{m}\Omega$ $\text{m}\Omega$ S μA μA μA
I_{DSS}	Zero gate voltage drain current	$V_{DS} = 55 \text{ V}; V_{GS} = 0 \text{ V}$	$T_j = 175^\circ\text{C}$	- - $T_j = 175^\circ\text{C}$	0.05 10 500	μA μA μA
$Q_{g(\text{tot})}$ Q_{gs} Q_{gd}	Total gate charge Gate-source charge Gate-drain (Miller) charge	$I_D = 50 \text{ A}; V_{DD} = 44 \text{ V}; V_{GS} = 5 \text{ V}$	- - -	27 4 14	- - -	nC nC nC
$t_{d\text{ on}}$ t_r $t_{d\text{ off}}$ t_f	Turn-on delay time Turn-on rise time Turn-off delay time Turn-off fall time	$V_{DD} = 30 \text{ V}; I_D = 25 \text{ A}; V_{GS} = 5 \text{ V}; R_G = 10 \Omega$ Resistive load	- - - -	30 80 95 40	45 130 135 55	ns ns ns ns
L_d L_d	Internal drain inductance Internal drain inductance	Measured from tab to centre of die Measured from drain lead to centre of die (SOT78 package only)	- -	3.5 4.5	- -	nH nH
L_s	Internal source inductance	Measured from source lead to source bond pad	-	7.5	-	nH
C_{iss} C_{oss} C_{rss}	Input capacitance Output capacitance Feedback capacitance	$V_{GS} = 0 \text{ V}; V_{DS} = 25 \text{ V}; f = 1 \text{ MHz}$	- - -	1500 300 150	2000 360 200	pF pF pF

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REVERSE DIODE LIMITING VALUES AND CHARACTERISTICS

$T_j = 25^\circ\text{C}$ unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I_s	Continuous source current (body diode)		-	-	50	A
I_{sm}	Pulsed source current (body diode)		-	-	200	A
V_{sd}	Diode forward voltage	$I_F = 25 \text{ A}; V_{GS} = 0 \text{ V}$ $I_F = 40 \text{ A}; V_{GS} = 0 \text{ V}$	-	0.95 1.0	1.2 -	V V
t_{rr} Q_{rr}	Reverse recovery time Reverse recovery charge	$I_F = 40 \text{ A}; -dI_F/dt = 100 \text{ A}/\mu\text{s};$ $V_{GS} = -10 \text{ V}; V_R = 30 \text{ V}$	-	40 0.07	- -	ns μC

AVALANCHE LIMITING VALUE

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
W_{DSS}	Drain-source non-repetitive unclamped inductive turn-off energy	$I_D = 40 \text{ A}; V_{DD} \leq 25 \text{ V}; V_{GS} = 5 \text{ V};$ $R_{GS} = 50 \Omega; T_{mb} = 25^\circ\text{C}$	-	80	mJ

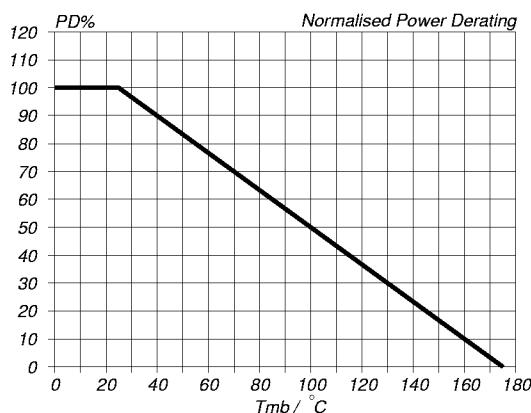


Fig.1. Normalised power dissipation.
 $PD\% = 100 \cdot P_D/P_{D\ 25\ ^\circ\text{C}} = f(T_{mb})$

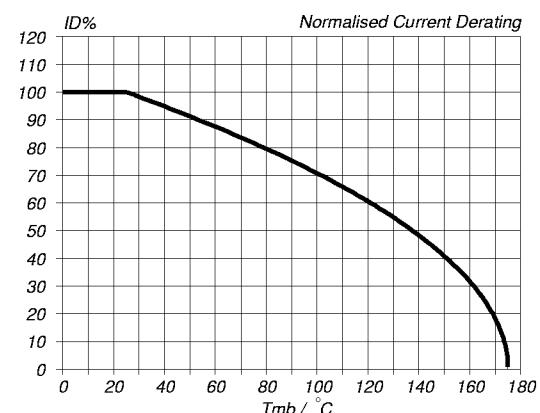


Fig.2. Normalised continuous drain current.
 $ID\% = 100 \cdot I_D/I_{D\ 25\ ^\circ\text{C}} = f(T_{mb}); \text{conditions: } V_{GS} \geq 5 \text{ V}$

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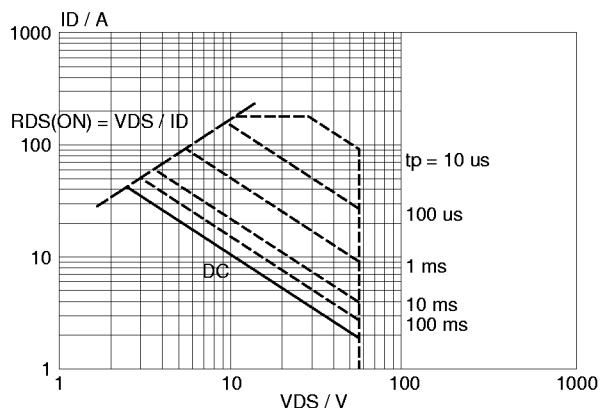


Fig.3. Safe operating area. $T_{mb} = 25^\circ\text{C}$
 I_D & $I_{DM} = f(V_{DS})$; I_{DM} single pulse; parameter t_p

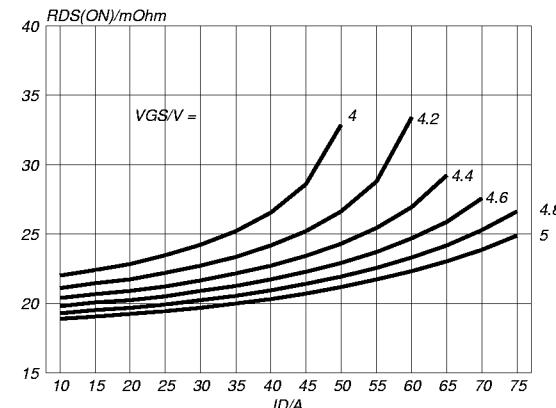


Fig.6. Typical on-state resistance, $T_j = 25^\circ\text{C}$.
 $R_{DS(ON)} = f(I_D)$; parameter V_{GS}

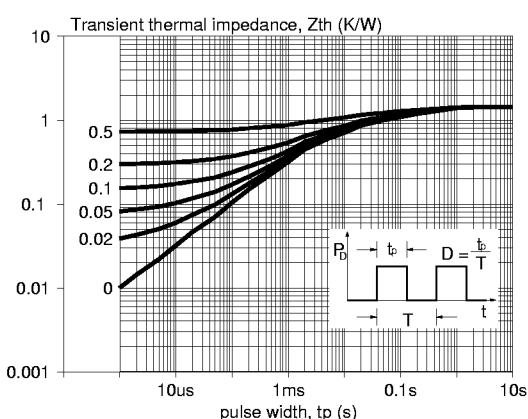


Fig.4. Transient thermal impedance.
 $Z_{th,j-mb} = f(t_p)$; parameter $D = t_p/T$

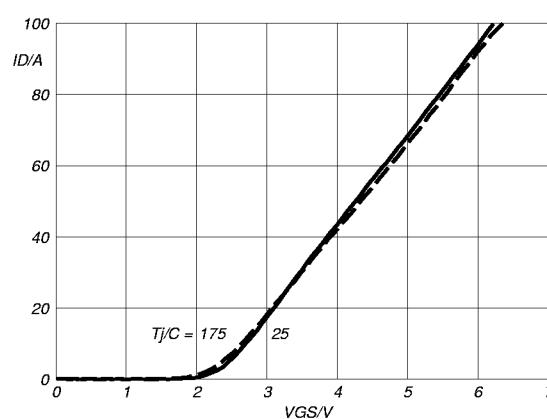


Fig.7. Typical transfer characteristics.
 $I_D = f(V_{GS})$; conditions: $V_{DS} = 25\text{ V}$; parameter T_j

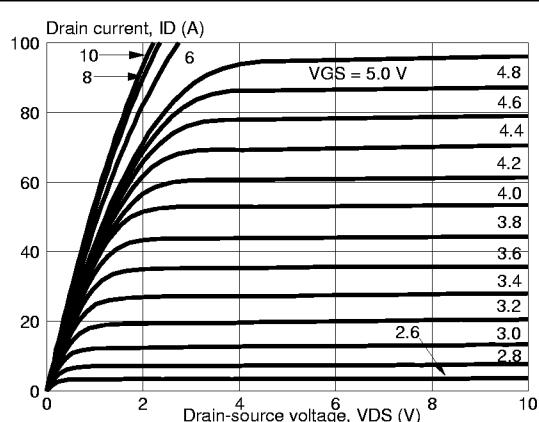


Fig.5. Typical output characteristics, $T_j = 25^\circ\text{C}$.
 $I_D = f(V_{DS})$; parameter V_{GS}

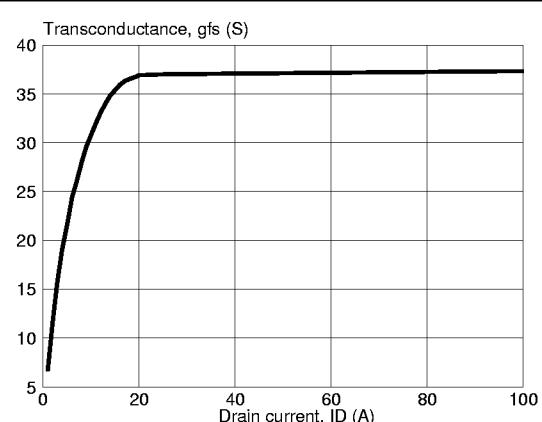


Fig.8. Typical transconductance, $T_j = 25^\circ\text{C}$.
 $g_{fs} = f(I_D)$; conditions: $V_{DS} = 25\text{ V}$

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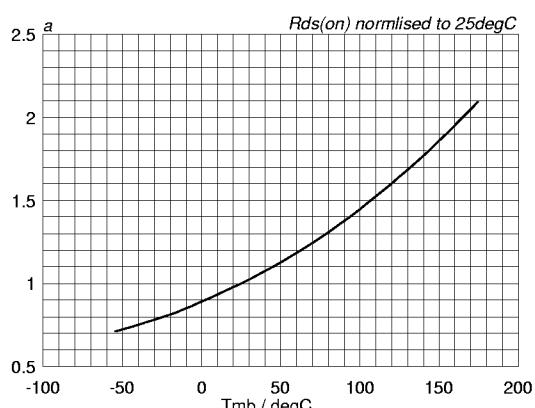


Fig.9. Normalised drain-source on-state resistance.
 $a = R_{DS(ON)}/R_{DS(ON)25}^{\circ C} = f(T_j); I_D = 25 \text{ A}; V_{GS} = 5 \text{ V}$

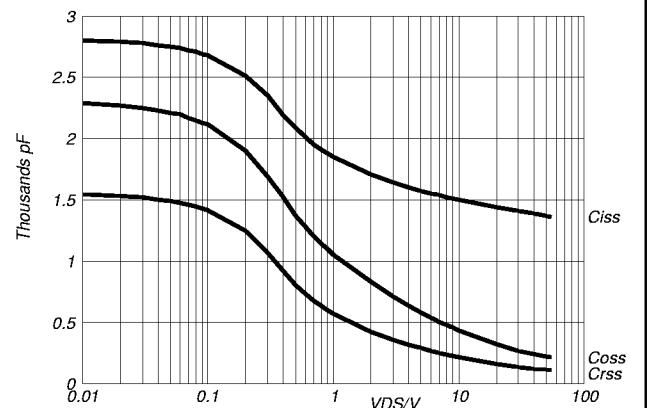


Fig.12. Typical capacitances, C_{iss} , C_{oss} , C_{rss} .
 $C = f(V_{DS})$; conditions: $V_{GS} = 0 \text{ V}; f = 1 \text{ MHz}$

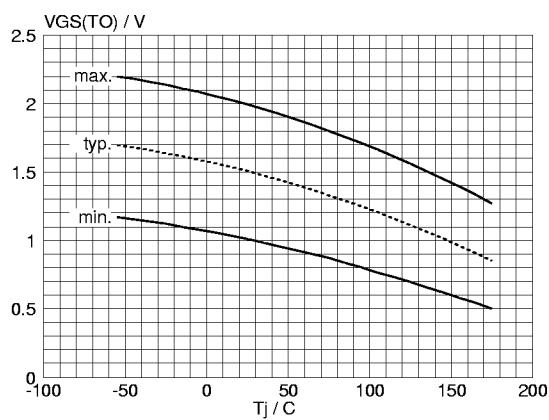


Fig.10. Gate threshold voltage.
 $V_{GS(TO)} = f(T_j)$; conditions: $I_D = 1 \text{ mA}; V_{DS} = V_{GS}$

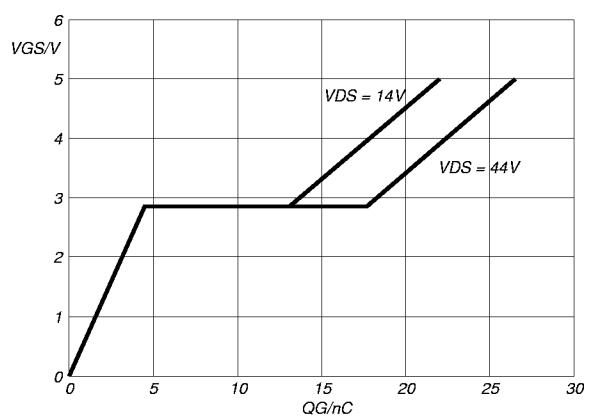


Fig.13. Typical turn-on gate-charge characteristics.
 $V_{GS} = f(Q_G)$; conditions: $I_D = 50 \text{ A}$; parameter V_{DS}

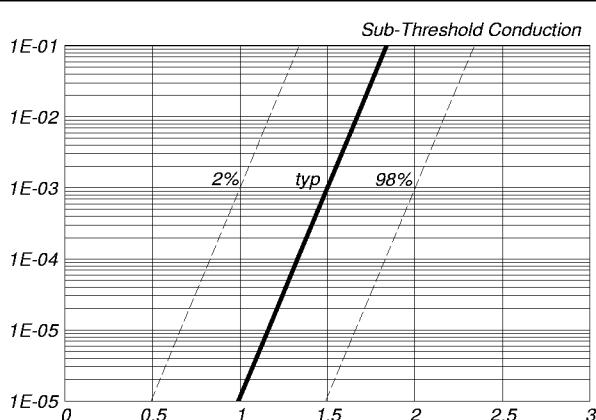


Fig.11. Sub-threshold drain current.
 $I_D = f(V_{GS})$; conditions: $T_j = 25^{\circ}\text{C}$; $V_{DS} = V_{GS}$

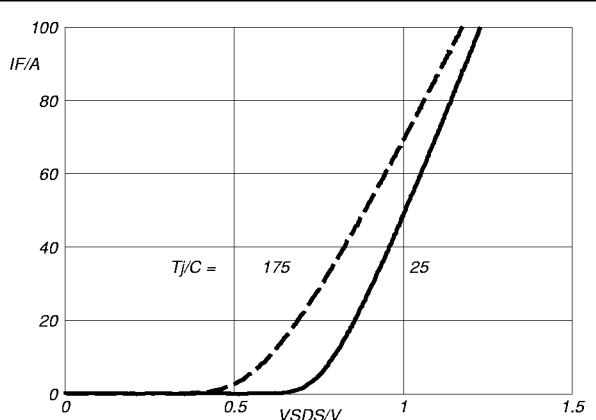


Fig.14. Typical reverse diode current.
 $I_F = f(V_{SDS})$; conditions: $V_{GS} = 0 \text{ V}$; parameter T_j

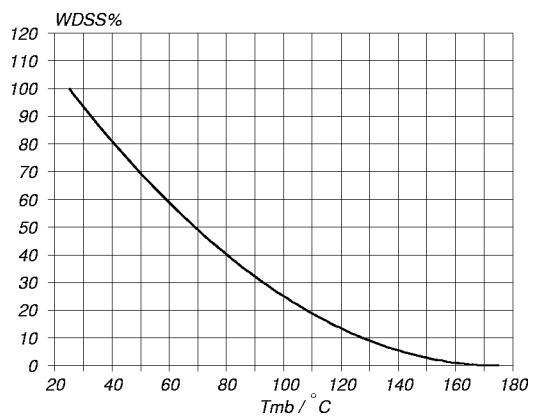
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Fig. 15. Normalised avalanche energy rating.
 $W_{DSS}\% = f(T_{mb})$; conditions: $I_D = 40\text{ A}$

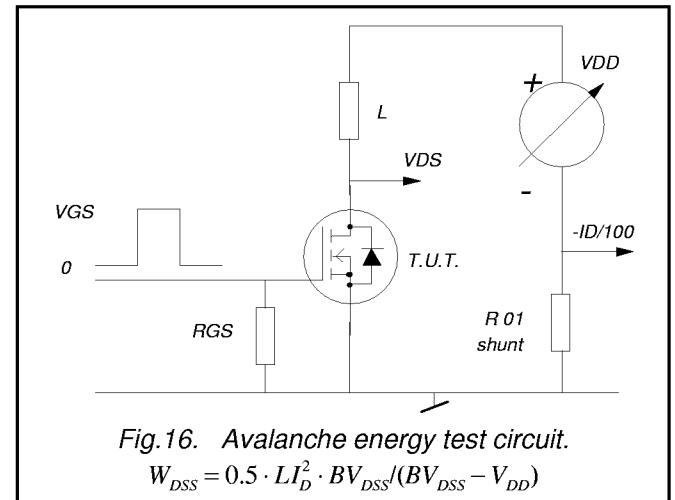


Fig. 16. Avalanche energy test circuit.
$$W_{DSS} = 0.5 \cdot L I_D^2 \cdot BV_{DSS} / (BV_{DSS} - V_{DD})$$

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MECHANICAL DATA

Dimensions in mm

Net Mass: 2 g

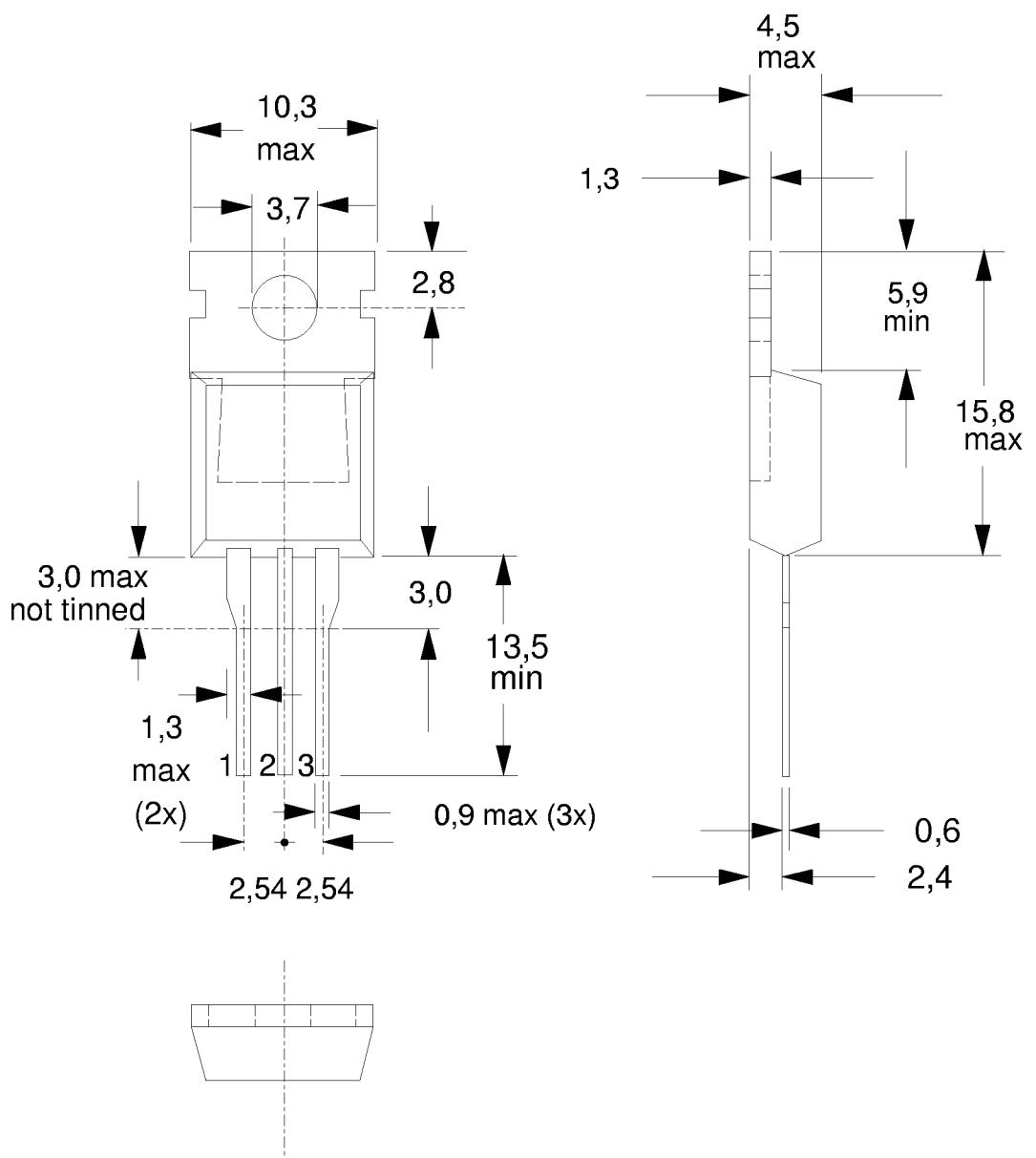


Fig.17. SOT78 (TO220AB); pin 2 connected to mounting base.

Notes

1. Observe the general handling precautions for electrostatic-discharge sensitive devices (ESDs) to prevent damage to MOS gate oxide.
2. Refer to mounting instructions for SOT78 (TO220) envelopes.
3. Epoxy meets UL94 V0 at 1/8".

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MECHANICAL DATA

Dimensions in mm

Net Mass: 1.4 g

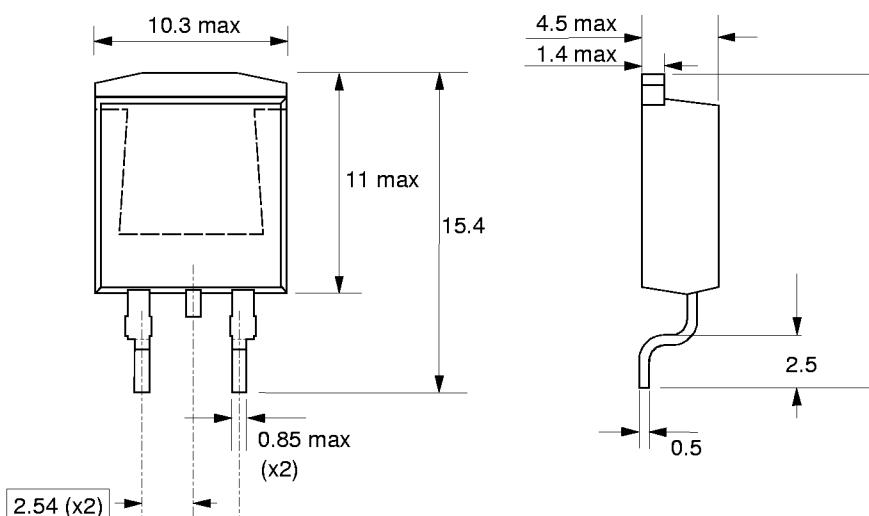


Fig.18. SOT404 : centre pin connected to mounting base.

MOUNTING INSTRUCTIONS

Dimensions in mm

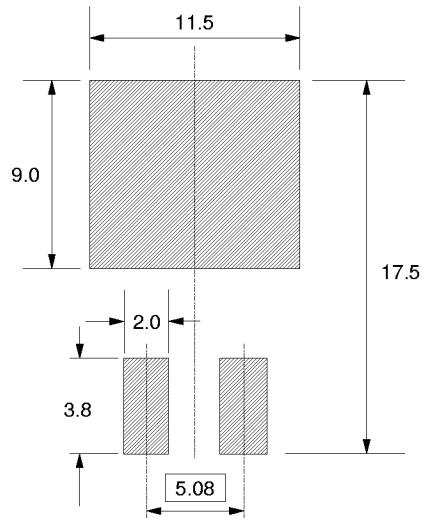


Fig.19. SOT404 : soldering pattern for surface mounting.

Notes

1. Observe the general handling precautions for electrostatic-discharge sensitive devices (ESDs) to prevent damage to MOS gate oxide.
2. Epoxy meets UL94 V0 at 1/8".

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MECHANICAL DATA

Dimensions in mm : Net Mass: 1.4 g

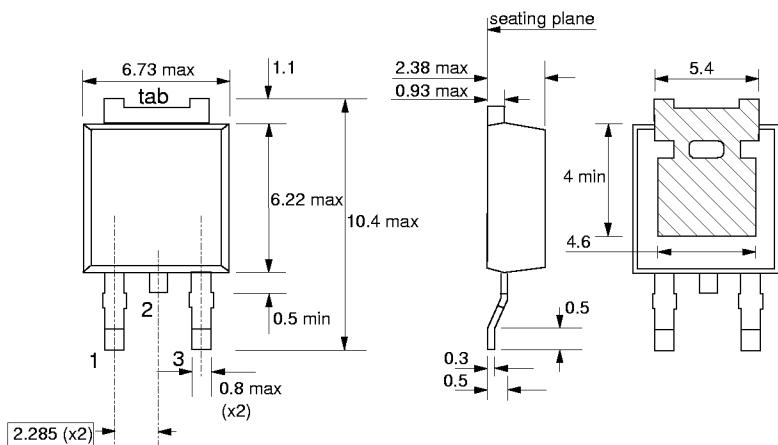


Fig.20. SOT428 : centre pin connected to mounting base.

MOUNTING INSTRUCTIONS

Dimensions in mm

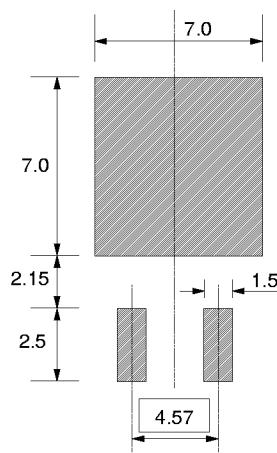


Fig.21. SOT428 : soldering pattern for surface mounting.

Notes

1. Observe the general handling precautions for electrostatic-discharge sensitive devices (ESDs) to prevent damage to MOS gate oxide.
2. Epoxy meets UL94 V0 at 1/8".