

## TL97x Output Rail-To-Rail Very-Low-Noise Operational Amplifiers

### 1 Features

- Rail-to-Rail Output Voltage Swing:  $\pm 2.4$  V at  $V_{CC} = \pm 2.5$  V
- Very Low Noise Level:  $4$  nV/ $\sqrt{\text{Hz}}$
- Ultra-Low Distortion: 0.003%
- High Dynamic Features: 12 MHz, 5 V/ $\mu\text{s}$
- Operating Range: 2.7 V to 12 V
- Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II
- ESD Performance Tested Per JESD 22
  - 2000-V Human-Body Model
  - 1500-V Charged-Device Model

### 2 Applications

- Portable Equipment
  - Music Players
  - Tablets
  - Cell Phones
- Instrumentation and Sensors
- Professional Audio Circuits

### 3 Description

The TL97x family of single, dual, and quad operational amplifiers operates at voltages as low as  $\pm 1.35$  V and features output rail-to-rail signal swing. The TL97x boast characteristics that make them particularly well suited for portable and battery-supplied equipment. Very low noise and low distortion characteristics make them ideal for audio preamplification.

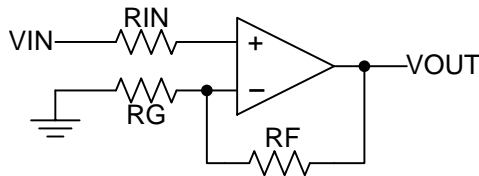
The TL971 is housed in the space-saving 5-pin SOT-23 package, which simplifies board design because of the ability to be placed anywhere (outside dimensions are 2.8 mm  $\times$  2.9 mm).

#### Device Information<sup>(1)</sup>

PART NUMBER	PACKAGE (PIN)	BODY SIZE (NOM)
TL971	SOIC (8)	4.90 mm $\times$ 3.90 mm
	SOT-23 (5)	2.80 mm $\times$ 2.90 mm
TL972	MSOP (8)	3.00 mm $\times$ 3.00 mm
	PDIP (8)	9.60 mm $\times$ 6.40 mm
	SOIC (8)	4.90 mm $\times$ 3.90 mm
	TSSOP (8)	3.00 mm $\times$ 4.40 mm
TL974	PDIP (14)	19.30 mm $\times$ 6.40 mm
	SOIC (14)	8.60 mm $\times$ 3.90 mm
	TSSOP (14)	5.00 mm $\times$ 4.40 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

### 4 Simplified Schematic



## Table of Contents

<b>1 Features</b> .....	<b>1</b>	8.2 Functional Block Diagram .....	<b>9</b>
<b>2 Applications</b> .....	<b>1</b>	8.3 Feature Description .....	<b>9</b>
<b>3 Description</b> .....	<b>1</b>	8.4 Device Functional Modes .....	<b>10</b>
<b>4 Simplified Schematic</b> .....	<b>1</b>	<b>9 Application and Implementation</b> .....	<b>11</b>
<b>5 Revision History</b> .....	<b>2</b>	9.1 Typical Application .....	<b>11</b>
<b>6 Pin Configuration and Functions</b> .....	<b>3</b>	<b>10 Power Supply Recommendations</b> .....	<b>13</b>
<b>7 Specifications</b> .....	<b>4</b>	<b>11 Layout</b> .....	<b>13</b>
7.1 Absolute Maximum Ratings .....	<b>4</b>	11.1 Layout Guidelines .....	<b>13</b>
7.2 ESD Ratings .....	<b>4</b>	11.2 Layout Example .....	<b>13</b>
7.3 Recommended Operating Conditions .....	<b>4</b>	<b>12 Device and Documentation Support</b> .....	<b>15</b>
7.4 Thermal Information .....	<b>4</b>	12.1 Related Links .....	<b>15</b>
7.5 Electrical Characteristics .....	<b>5</b>	12.2 Trademarks .....	<b>15</b>
7.6 Typical Characteristics .....	<b>5</b>	12.3 Electrostatic Discharge Caution .....	<b>15</b>
<b>8 Detailed Description</b> .....	<b>9</b>	12.4 Glossary .....	<b>15</b>
8.1 Overview .....	<b>9</b>	<b>13 Mechanical, Packaging, and Orderable Information</b> .....	<b>15</b>

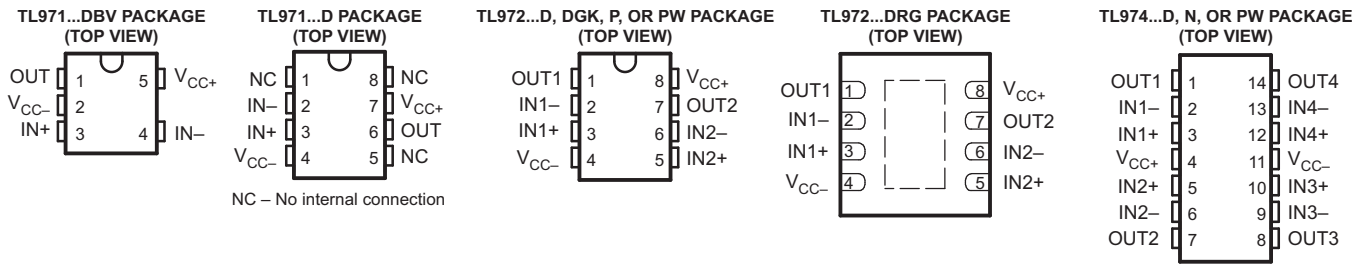
## 5 Revision History

<b>Changes from Revision G (May 2012) to Revision H</b>	<b>Page</b>
• Added <i>Applications</i> , <i>Device Information</i> table, <i>Pin Functions</i> table, <i>ESD Ratings</i> table, <i>Thermal Information</i> table, <i>Typical Characteristics</i> , <i>Feature Description</i> section, <i>Device Functional Modes</i> , <i>Application and Implementation</i> section, <i>Power Supply Recommendations</i> section, <i>Layout</i> section, <i>Device and Documentation Support</i> section, and <i>Mechanical, Packaging, and Orderable Information</i> section. ....	<b>1</b>
• Deleted <i>Ordering Information</i> table. ....	<b>1</b>

<b>Changes from Revision F (December 2009) to Revision G</b>	<b>Page</b>
• Changed slew rate MIN value. ....	<b>5</b>

## 6 Pin Configuration and Functions



### Pin Functions

NAME	PIN					TYPE	DESCRIPTION
	TL971	TL971	TL972		TL974		
	DBV	D	D, DGK, P, PW	DRG	D, N, PW		
IN+	3	3	—	—	—	I	Noninverting input
IN-	4	2	—	—	—	I	Inverting input
IN1+	—	—	3	3	3	I	Noninverting input
IN1-	—	—	2	2	2	I	Inverting input
IN2+	—	—	5	5	5	I	Noninverting input
IN2-	—	—	6	6	6	I	Inverting input
IN3+	—	—	—	—	10	I	Noninverting input
IN3-	—	—	—	—	9	I	Inverting input
IN4+	—	—	—	—	12	I	Noninverting input
IN4-	—	—	—	—	13	I	Inverting input
NC	—	1	—	—	—	—	No Connect
		5					
		8					
OUT	1	6	—	—	—	O	Output
OUT1	—	—	1	1	1	O	Output
OUT2	—	—	7	7	7	O	Output
OUT3	—	—	—	—	8	O	Output
OUT4	—	—	—	—	14	O	Output
V <sub>CC+</sub>	5	7	8	8	4	-	Positive supply
V <sub>CC-</sub>	2	4	4	4	11	-	Negative supply

## 7 Specifications

### 7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)<sup>(1)</sup>

		MIN	MAX	UNIT
V <sub>CC</sub>	Supply voltage range	2.7	15	V
V <sub>ID</sub>	Differential input voltage <sup>(2)</sup>	±1 V		V
V <sub>IN</sub>	Input voltage range <sup>(3)</sup>	V <sub>CC-</sub> – 0.3	V <sub>CC+</sub> + 0.3	V
T <sub>J</sub>	Maximum junction temperature	150		°C
T <sub>stg</sub>	Storage temperature range	–65	150	°C

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) Differential voltages for the noninverting input terminal are with respect to the inverting input terminal.
- (3) The input and output voltages must never exceed V<sub>CC</sub> + 0.3 V.

### 7.2 ESD Ratings

		VALUE	UNIT
V <sub>(ESD)</sub>	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins <sup>(1)</sup>	2000
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins <sup>(2)</sup>	1500

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
- (2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

### 7.3 Recommended Operating Conditions

		MIN	MAX	UNIT
V <sub>CC</sub>	Supply voltage	2.7	12	V
V <sub>ICM</sub>	Common-mode input voltage	V <sub>CC-</sub> + 1.15	V <sub>CC+</sub> – 1.15	V
T <sub>A</sub>	Operating free-air temperature	–40	125	°C

### 7.4 Thermal Information

THERMAL METRIC <sup>(1)</sup>	TL971		TL972					TL974			UNIT	
	D <sup>(2)</sup>	DBV <sup>(2)</sup>	D <sup>(2)</sup>	DGK <sup>(3)</sup>	DRG <sup>(3)</sup>	P <sup>(2)</sup>	PW <sup>(2)</sup>	D <sup>(2)</sup>	N <sup>(2)</sup>	PW <sup>(2)</sup>		
	8 PINS	5 PINS	8 PINS					14 PINS				
R <sub>θJA</sub>	Package thermal impedance, junction to free air	97	206	97	172	44	85	149	86	80	113	°C/W

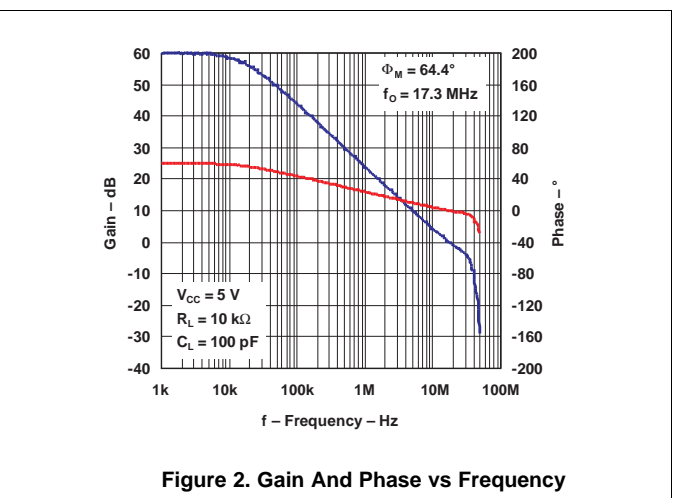
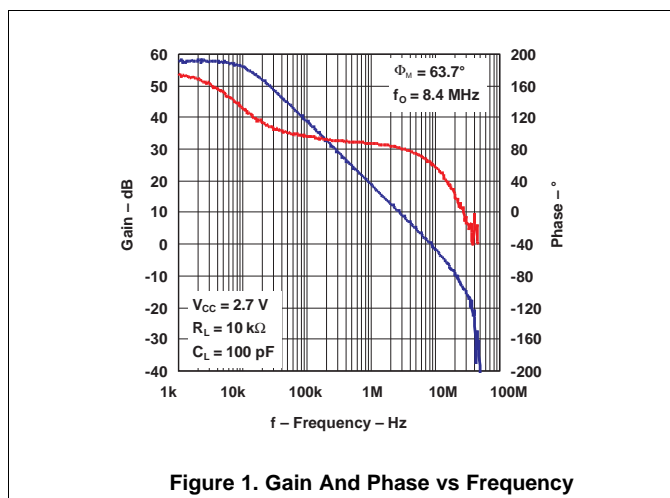
- (1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report ([SPRA953](#)).
- (2) Package thermal impedance is calculated in accordance with JESD 51-7.
- (3) Package thermal impedance is calculated in accordance with JESD 51-5.

## 7.5 Electrical Characteristics

 $V_{CC+} = 2.5\text{ V}$ ,  $V_{CC-} = -2.5\text{ V}$ , full-range  $T_A = -40^\circ\text{C}$  to  $125^\circ\text{C}$  (unless otherwise noted)

PARAMETER		TEST CONDITIONS	$T_A$	MIN	TYP	MAX	UNIT
$V_{IO}$	Input offset voltage		25°C		1	4	mV
			Full range			6	
$\alpha V_{IO}$	Input offset voltage drift	$V_{ICM} = 0\text{ V}$ , $V_O = 0\text{ V}$	25°C		5		$\mu\text{V}/^\circ\text{C}$
$I_{IO}$	Input offset current	$V_{ICM} = 0\text{ V}$ , $V_O = 0\text{ V}$	25°C		10	150	nA
$I_{IB}$	Input bias current	$V_{ICM} = 0\text{ V}$ , $V_O = 0\text{ V}$	25°C		200	750	nA
			Full range			1000	
$V_{ICM}$	Common-mode input voltage		25°C	-1.35		1.35	V
CMRR	Common-mode rejection ratio	$V_{ICM} = \pm 1.35\text{ V}$	25°C	60	85		dB
SVR	Supply-voltage rejection ratio	$V_{CC} = \pm 2\text{ V}$ to $\pm 3\text{ V}$	25°C	60	70		dB
$A_{VD}$	Large-signal voltage gain	$R_L = 2\text{ k}\Omega$	25°C	70	80		dB
$V_{OH}$	High-level output voltage	$R_L = 2\text{ k}\Omega$	25°C	2	2.4		V
$V_{OL}$	Low-level output voltage	$R_L = 2\text{ k}\Omega$	25°C		-2.4	-2	V
$I_{source}$	Output source current	$V_{OUT} = \pm 2.5\text{ V}$	25°C	1.2	1.4		mA
			Full range		1		
$I_{sink}$	Output sink current	$V_{OUT} = \pm 2.5\text{ V}$	25°C	50	80		mA
			Full range		25		
$I_{CC}$	Supply current (per amplifier)	Unity gain, No load	25°C		2	2.8	mA
			Full range			3.2	
GBWP	Gain bandwidth product	$f = 100\text{ kHz}$ , $R_L = 2\text{ k}\Omega$ , $C_L = 100\text{ pF}$	25°C	8.5	12		MHz
SR	Slew rate	$A_V = 1$ , $V_{IN} = \pm 1\text{ V}$	25°C	2.8	5		V/ $\mu\text{s}$
			Full range		2.8		
$\Phi_m$	Phase margin at unity gain	$R_L = 2\text{ k}\Omega$ , $C_L = 100\text{ pF}$	25°C		60		$^\circ$
Gm	Gain margin	$R_L = 2\text{ k}\Omega$ , $C_L = 100\text{ pF}$	25°C		10		dB
$V_n$	Equivalent input noise voltage	$f = 100\text{ kHz}$	25°C		4		$\text{nV}/\sqrt{\text{Hz}}$
THD	Total harmonic distortion	$f = 1\text{ kHz}$ , $A_V = -1$ , $R_L = 10\text{ k}\Omega$	25°C		0.003		%

## 7.6 Typical Characteristics



Typical Characteristics (continued)

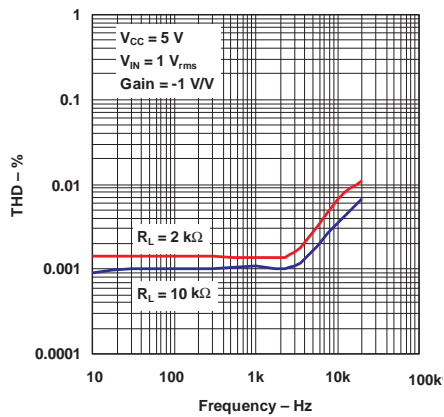


Figure 3. Total Harmonic Distortion vs Frequency

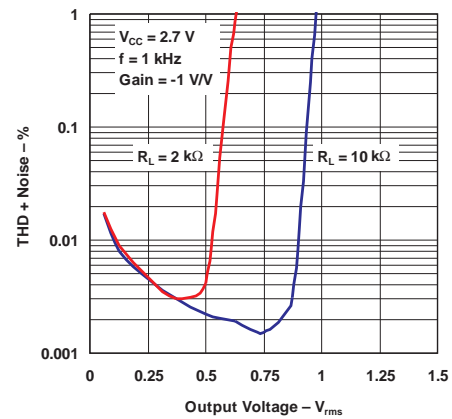


Figure 4. Total Harmonic Distortion + Noise vs Output Voltage

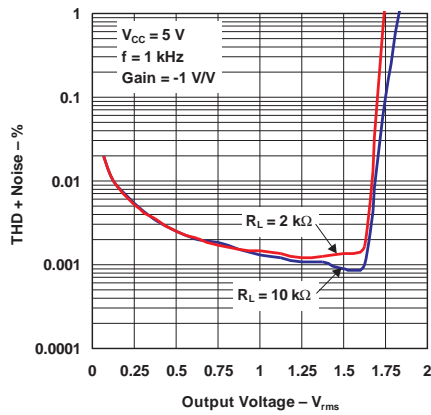


Figure 5. Total Harmonic Distortion + Noise vs Output Voltage

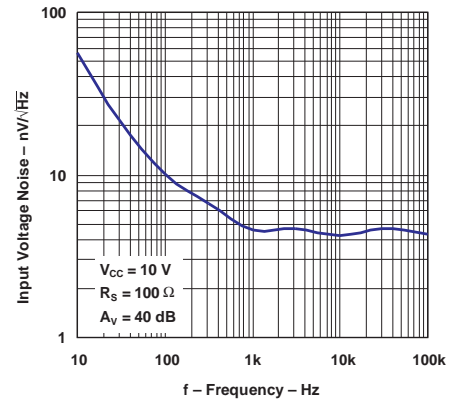


Figure 6. Input Voltage Noise vs Frequency

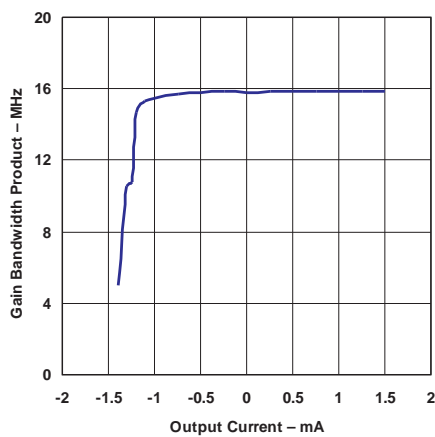


Figure 7. Gain Bandwidth Product vs Output Current

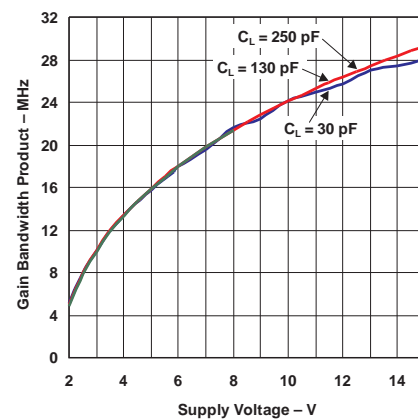


Figure 8. Gain Bandwidth Product vs Supply Voltage

Typical Characteristics (continued)

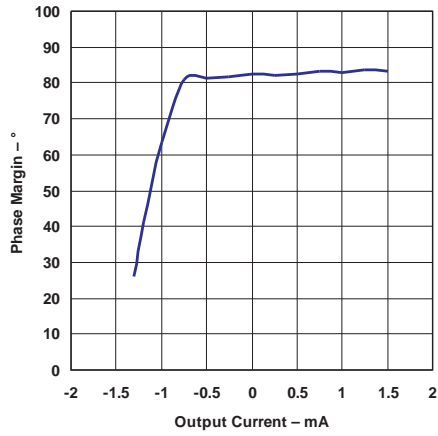


Figure 9. Phase Margin vs Output Current

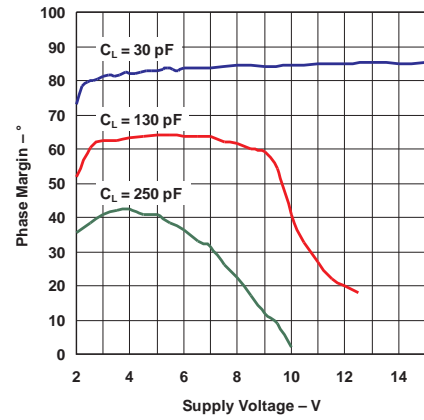


Figure 10. Phase Margin vs Supply Voltage

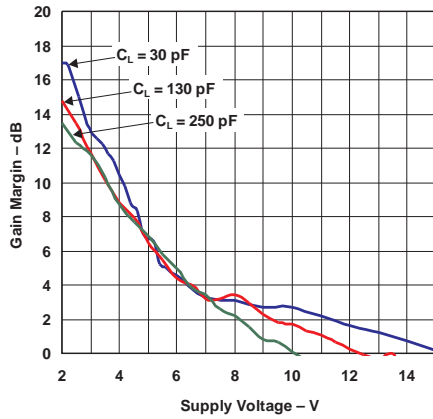


Figure 11. Gain Margin vs Supply Voltage

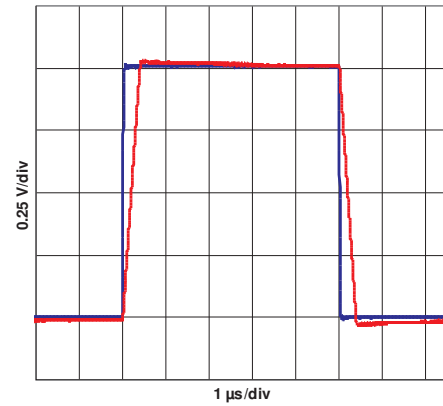


Figure 12. Input Response

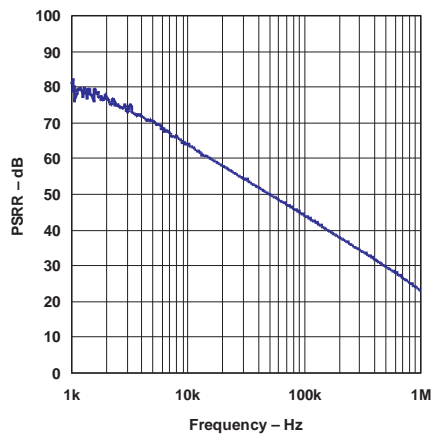


Figure 13. Power-Supply Ripple Rejection vs Frequency

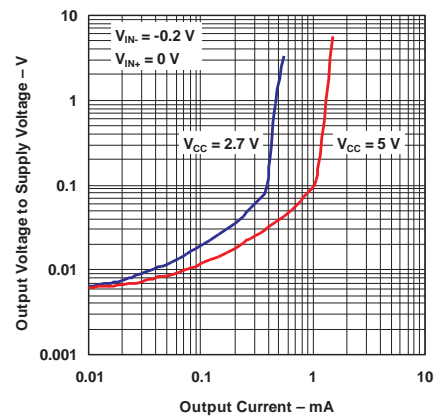
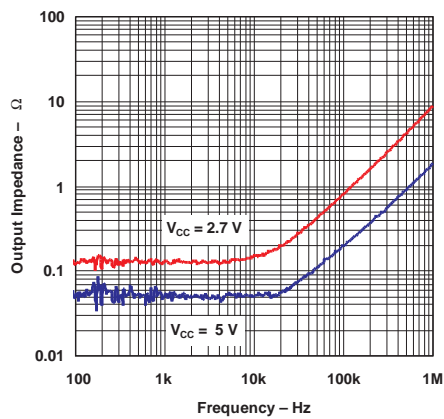
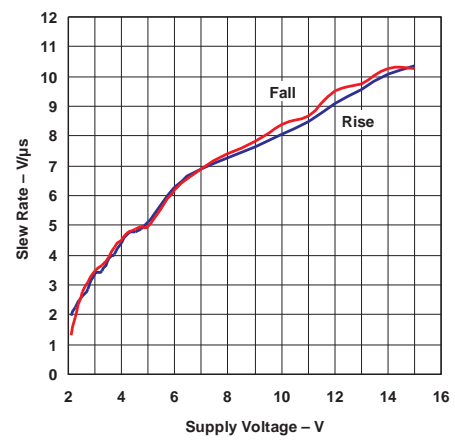


Figure 14. Output Voltage vs Output Current

**Typical Characteristics (continued)**



**Figure 15. Output Impedance vs Frequency**



**Figure 16. Slew Rate vs Supply Voltage**



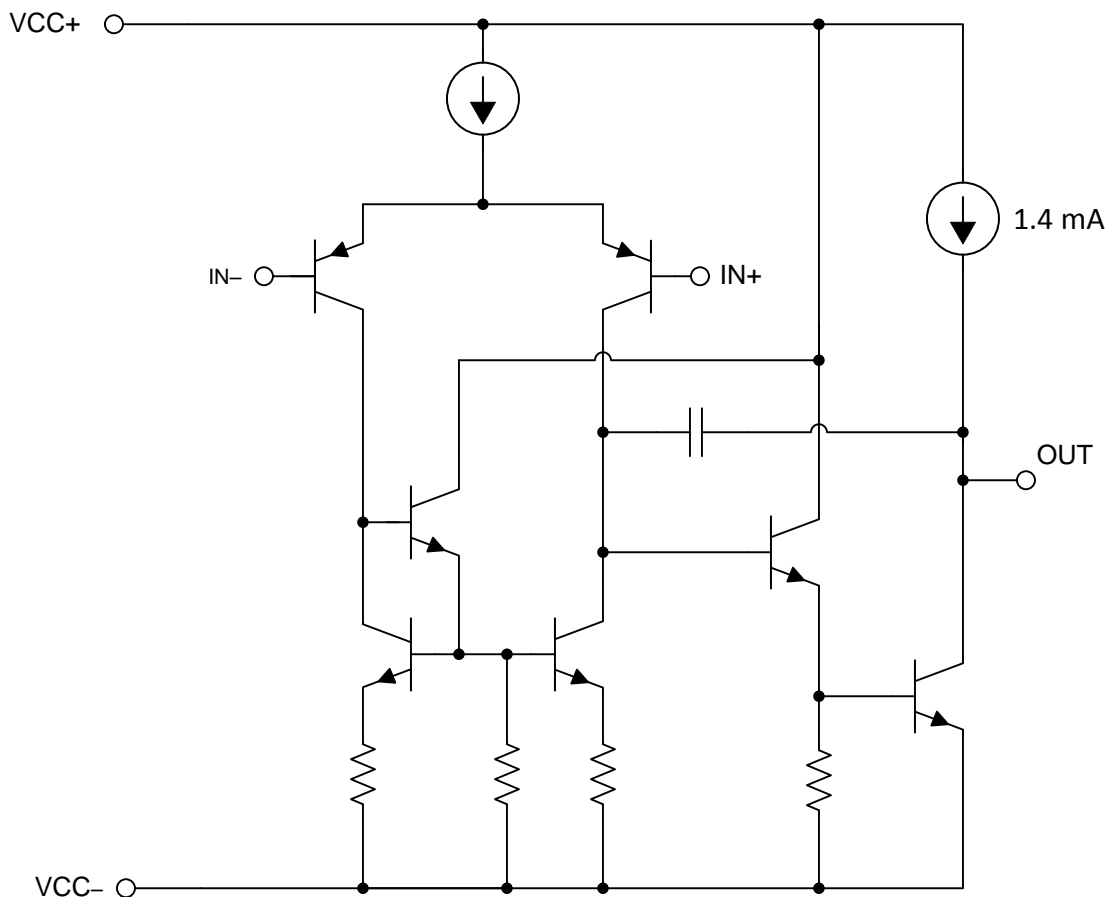
## 8 Detailed Description

### 8.1 Overview

The TL97x family of operational amplifiers operates at voltages as low as  $\pm 1.35$  V and features output rail-to-rail signal swing. The TL97x boast characteristics that make them particularly well suited for portable and battery-supplied equipment. Very low noise and low distortion characteristics make them ideal for audio preamplification. The TL97x family comes in single, dual, and quad operational amplifier packages of varying sizes.

The TL971 is housed in the space-saving 5-pin SOT-23 package, which simplifies board design because of the ability to be placed anywhere (outside dimensions are 2.8 mm  $\times$  2.9 mm).

### 8.2 Functional Block Diagram



### 8.3 Feature Description

#### 8.3.1 Slew Rate

The slew rate is the rate at which an operational amplifier can change its output when there is a change on the input. The TL97x devices have a 5 V/ $\mu$ s slew rate.

#### 8.3.2 Unity-Gain Bandwidth

The unity-gain bandwidth is the frequency up to which an amplifier with a unity gain may be operated without greatly distorting the signal. The TL97x devices have a 12-MHz unity-gain bandwidth.

## Feature Description (continued)

### 8.3.3 Low Total Harmonic Distortion

Harmonic distortions to an audio signal are created by electronic components in a circuit. Total harmonic distortion (THD) is a measure of harmonic distortions accumulated by a signal in an audio system. The TL97x devices have a very low THD of 0.003% meaning that they will add little harmonic distortion when used in audio signal applications.

### 8.3.4 Operating Voltage

The TL97x devices are fully specified and ensured for operation from 2.7 V to 12 V. In addition, many specifications apply from  $-40^{\circ}\text{C}$  to  $125^{\circ}\text{C}$ .

## 8.4 Device Functional Modes

The TL97x devices are powered on when the supply is connected. Each of these devices can be operated as a single supply operational amplifier or dual supply amplifier depending on the application.

## 9 Application and Implementation

### NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

### 9.1 Typical Application

The voltage follower configuration of the operational amplifier is used for applications where a weak signal is used to drive a relatively high current load. This circuit is also called a buffer amplifier or unity gain amplifier. The inputs of an operational amplifier have a very high resistance which puts a negligible current load on the voltage source. The output resistance of the operational amplifier is almost negligible, so it can provide as much current as necessary to the output load.

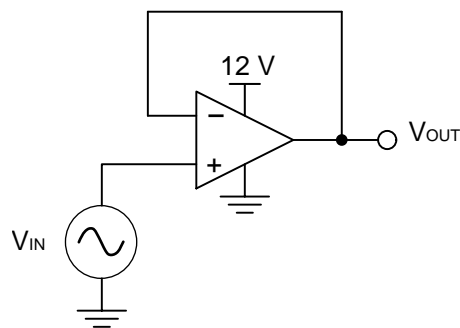


Figure 17. Voltage follower schematic

#### 9.1.1 Design Requirements

- Input at positive Terminal
- Output range of 0 V to 12 V
- Input range of 0 V to 12 V
- Short-circuit feedback to negative input for unity gain

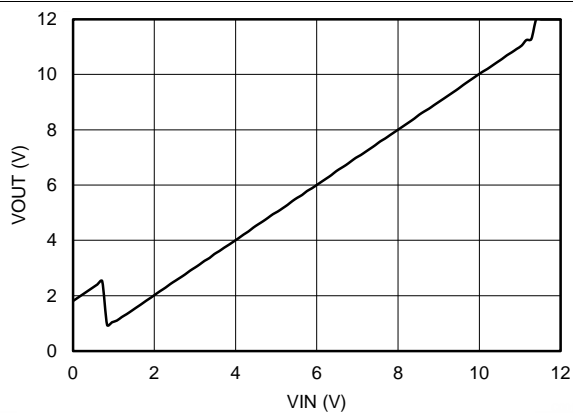
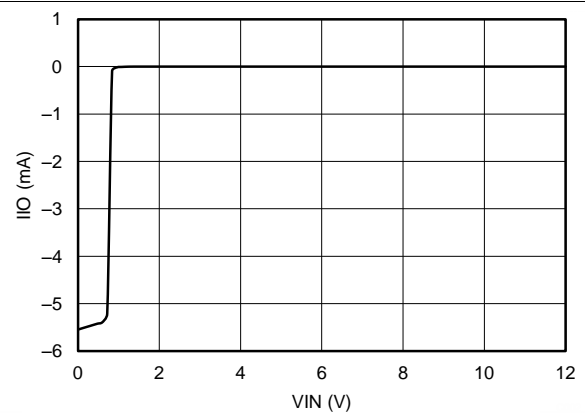
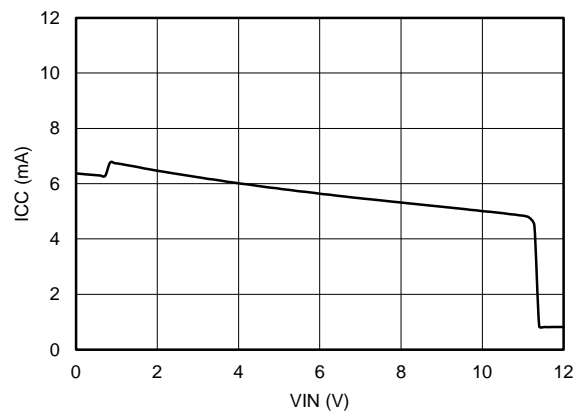
#### 9.1.2 Detailed Design Procedure

##### 9.1.2.1 Output Voltage Swing

The output voltage of an operational amplifier is limited by its internal circuitry to some level below the supply rails. For this amplifier, the output voltage must be within  $\pm 12$  V.

##### 9.1.2.2 Supply and Input Voltage

For correct operation of the amplifier, neither input must be higher than the recommended positive supply rail voltage or lower than the recommended negative supply rail voltage. The chosen amplifier must be able to operate at the supply voltage that accommodates the inputs. Because the input for this application goes up to 12 V, the supply voltage must be 15 V. Using a negative voltage on the lower rail rather than ground, allows the amplifier to maintain linearity for the full range of inputs.

**Typical Application (continued)**
**9.1.3 Application Curves for Output Characteristics**

**Figure 18. Output Voltage vs Input Voltage**

**Figure 19. Current Drawn by Input of Voltage Follower ( $I_{IO}$ ) vs Input Voltage**

**Figure 20. Current Drawn from Supply ( $I_{CC}$ ) vs Input Voltage**

## 10 Power Supply Recommendations

The TL97x devices are specified for operation from 2.7 to 12 V; many specifications apply from -40 °C to 125 °C.

### CAUTION

Supply voltages larger than 15 V can permanently damage the device (see the [Absolute Maximum Ratings](#)).

Place 0.1- $\mu$ F bypass capacitors close to the power-supply pins to reduce errors coupling in from noisy or high impedance power supplies. For more detailed information on bypass capacitor placement, refer to the [Layout Guidelines](#).

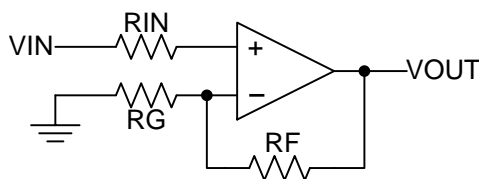
## 11 Layout

### 11.1 Layout Guidelines

For best operational performance of the device, use good PCB layout practices, including:

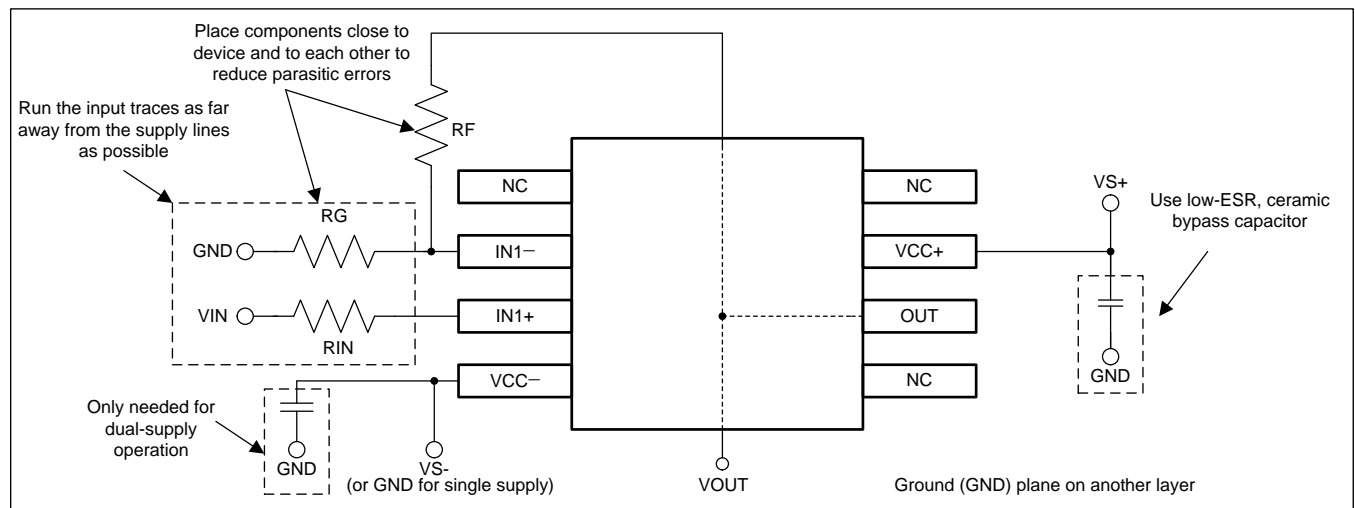
- Noise can propagate into analog circuitry through the power pins of the circuit as a whole and the operational amplifier. Bypass capacitors are used to reduce the coupled noise by providing low impedance power sources local to the analog circuitry.
  - Connect low-ESR, 0.1- $\mu$ F ceramic bypass capacitors between each supply pin and ground, placed as close to the device as possible. A single bypass capacitor from V+ to ground is applicable for single supply applications.
- Separate grounding for analog and digital portions of circuitry is one of the simplest and most-effective methods of noise suppression. One or more layers on multilayer PCBs are usually devoted to ground planes. A ground plane helps distribute heat and reduces EMI noise pickup. Make sure to physically separate digital and analog grounds, paying attention to the flow of the ground current. For more detailed information, refer to Circuit Board Layout Techniques, [SLOA089](#).
- To reduce parasitic coupling, run the input traces as far away from the supply or output traces as possible. If it is not possible to keep them separate, it is much better to cross the sensitive trace perpendicular as opposed to in parallel with the noisy trace.
- Place the external components as close to the device as possible. Keeping RF and RG close to the inverting input minimizes parasitic capacitance, as shown in [Layout Example](#).
- Keep the length of input traces as short as possible. Always remember that the input traces are the most sensitive part of the circuit.
- Consider a driven, low-impedance guard ring around the critical traces. A guard ring can significantly reduce leakage currents from nearby traces that are at different potentials.

### 11.2 Layout Example



**Figure 21. Operational Amplifier Schematic for Noninverting Configuration**

**Layout Example (continued)**



**Figure 22. Operational Amplifier Board Layout for Noninverting Configuration**

## 12 Device and Documentation Support

### 12.1 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

**Table 1. Related Links**

PARTS	PRODUCT FOLDER	SAMPLE & BUY	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
TL971	<a href="#">Click here</a>	<a href="#">Click here</a>	<a href="#">Click here</a>	<a href="#">Click here</a>	<a href="#">Click here</a>
TL972	<a href="#">Click here</a>	<a href="#">Click here</a>	<a href="#">Click here</a>	<a href="#">Click here</a>	<a href="#">Click here</a>
TL974	<a href="#">Click here</a>	<a href="#">Click here</a>	<a href="#">Click here</a>	<a href="#">Click here</a>	<a href="#">Click here</a>

### 12.2 Trademarks

All trademarks are the property of their respective owners.

### 12.3 Electrostatic Discharge Caution



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

### 12.4 Glossary

[SLYZ022](#) — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.



## 13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TL971ID	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	Z971	<a href="#">Samples</a>
TL971IDR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	Z971	<a href="#">Samples</a>
TL971IDRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	Z971	<a href="#">Samples</a>
TL972ID	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	Z972	<a href="#">Samples</a>
TL972IDGKR	ACTIVE	VSSOP	DGK	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	TSA	<a href="#">Samples</a>
TL972IDR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	Z972	<a href="#">Samples</a>
TL972IDRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	Z972	<a href="#">Samples</a>
TL972IP	ACTIVE	PDIP	P	8	50	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	-40 to 125	TL972IP	<a href="#">Samples</a>
TL972IPE4	ACTIVE	PDIP	P	8	50	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	-40 to 125	TL972IP	<a href="#">Samples</a>
TL972IPW	ACTIVE	TSSOP	PW	8	150	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	Z972	<a href="#">Samples</a>
TL972IPWR	ACTIVE	TSSOP	PW	8	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	Z972	<a href="#">Samples</a>
TL972IPWRG4	ACTIVE	TSSOP	PW	8	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	Z972	<a href="#">Samples</a>
TL974ID	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	TL974I	<a href="#">Samples</a>
TL974IDG4	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	TL974I	<a href="#">Samples</a>
TL974IDR	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	TL974I	<a href="#">Samples</a>
TL974IN	ACTIVE	PDIP	N	14	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	-40 to 125	TL974IN	<a href="#">Samples</a>
TL974INE4	ACTIVE	PDIP	N	14	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	-40 to 125	TL974IN	<a href="#">Samples</a>



Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TL974IPW	ACTIVE	TSSOP	PW	14	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	Z974	
TL974IPWR	ACTIVE	TSSOP	PW	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	Z974	

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

**Important Information and Disclaimer:** The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

**OTHER QUALIFIED VERSIONS OF TL971, TL972, TL974 :**

- Automotive: [TL971-Q1](#), [TL972-Q1](#), [TL974-Q1](#)

## NOTE: Qualified Version Definitions:

- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

**TAPE AND REEL INFORMATION**

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TL971IDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TL972IDGKR	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
TL972IDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TL972IPWR	TSSOP	PW	8	2000	330.0	12.4	7.0	3.6	1.6	8.0	12.0	Q1
TL974IDR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
TL974IPWR	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

**TAPE AND REEL BOX DIMENSIONS**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TL971IDR	SOIC	D	8	2500	340.5	338.1	20.6
TL972IDGKR	VSSOP	DGK	8	2500	358.0	335.0	35.0
TL972IDR	SOIC	D	8	2500	340.5	338.1	20.6
TL972IPWR	TSSOP	PW	8	2000	367.0	367.0	35.0
TL974IDR	SOIC	D	14	2500	333.2	345.9	28.6
TL974IPWR	TSSOP	PW	14	2000	367.0	367.0	35.0

P (R-PDIP-T8)

PLASTIC DUAL-IN-LINE PACKAGE



- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - C. Falls within JEDEC MS-001 variation BA.

N (R-PDIP-T\*\*)

PLASTIC DUAL-IN-LINE PACKAGE

16 PINS SHOWN



- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - $\triangle C$  Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
  - $\triangle D$  The 20 pin end lead shoulder width is a vendor option, either half or full width.

DGK (S-PDSO-G8)

PLASTIC SMALL-OUTLINE PACKAGE



- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 per end.
  - D. Body width does not include interlead flash. Interlead flash shall not exceed 0.50 per side.
  - E. Falls within JEDEC MO-187 variation AA, except interlead flash.

D (R-PDSO-G14)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
  - Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
  - E. Reference JEDEC MS-012 variation AB.



D (R-PDSO-G14)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Publication IPC-7351 is recommended for alternate designs.
  - D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
  - E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.



PW (R-PDSO-G14)

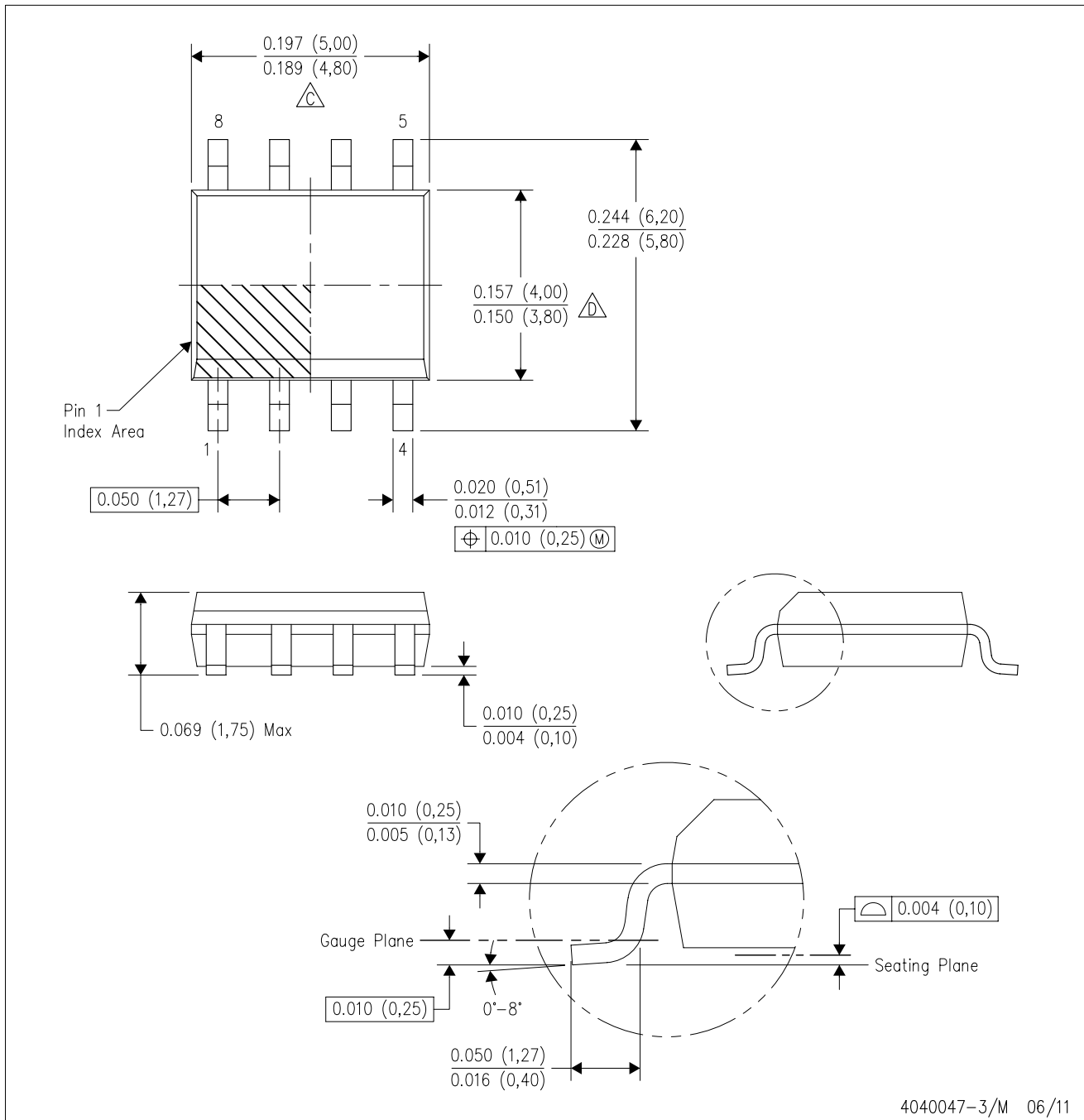
PLASTIC SMALL OUTLINE





- NOTES:
- All linear dimensions are in millimeters.
  - This drawing is subject to change without notice.
  - Publication IPC-7351 is recommended for alternate designs.
  - Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
  - Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

D (R-PDSO-G8)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  -  Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
  -  Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
  - E. Reference JEDEC MS-012 variation AA.

D (R-PDSO-G8)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Publication IPC-7351 is recommended for alternate designs.
  - D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
  - E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.



## IMPORTANT NOTICE

Texas Instruments Incorporated and its subsidiaries (TI) reserve the right to make corrections, enhancements, improvements and other changes to its semiconductor products and services per JESD46, latest issue, and to discontinue any product or service per JESD48, latest issue. Buyers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All semiconductor products (also referred to herein as "components") are sold subject to TI's terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its components to the specifications applicable at the time of sale, in accordance with the warranty in TI's terms and conditions of sale of semiconductor products. Testing and other quality control techniques are used to the extent TI deems necessary to support this warranty. Except where mandated by applicable law, testing of all parameters of each component is not necessarily performed.

TI assumes no liability for applications assistance or the design of Buyers' products. Buyers are responsible for their products and applications using TI components. To minimize the risks associated with Buyers' products and applications, Buyers should provide adequate design and operating safeguards.

TI does not warrant or represent that any license, either express or implied, is granted under any patent right, copyright, mask work right, or other intellectual property right relating to any combination, machine, or process in which TI components or services are used. Information published by TI regarding third-party products or services does not constitute a license to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

Reproduction of significant portions of TI information in TI data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. TI is not responsible or liable for such altered documentation. Information of third parties may be subject to additional restrictions.

Resale of TI components or services with statements different from or beyond the parameters stated by TI for that component or service voids all express and any implied warranties for the associated TI component or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

Buyer acknowledges and agrees that it is solely responsible for compliance with all legal, regulatory and safety-related requirements concerning its products, and any use of TI components in its applications, notwithstanding any applications-related information or support that may be provided by TI. Buyer represents and agrees that it has all the necessary expertise to create and implement safeguards which anticipate dangerous consequences of failures, monitor failures and their consequences, lessen the likelihood of failures that might cause harm and take appropriate remedial actions. Buyer will fully indemnify TI and its representatives against any damages arising out of the use of any TI components in safety-critical applications.

In some cases, TI components may be promoted specifically to facilitate safety-related applications. With such components, TI's goal is to help enable customers to design and create their own end-product solutions that meet applicable functional safety standards and requirements. Nonetheless, such components are subject to these terms.

No TI components are authorized for use in FDA Class III (or similar life-critical medical equipment) unless authorized officers of the parties have executed a special agreement specifically governing such use.

Only those TI components which TI has specifically designated as military grade or "enhanced plastic" are designed and intended for use in military/aerospace applications or environments. Buyer acknowledges and agrees that any military or aerospace use of TI components which have **not** been so designated is solely at the Buyer's risk, and that Buyer is solely responsible for compliance with all legal and regulatory requirements in connection with such use.

TI has specifically designated certain components as meeting ISO/TS16949 requirements, mainly for automotive use. In any case of use of non-designated products, TI will not be responsible for any failure to meet ISO/TS16949.

### Products

Audio	<a href="http://www.ti.com/audio">www.ti.com/audio</a>
Amplifiers	<a href="http://amplifier.ti.com">amplifier.ti.com</a>
Data Converters	<a href="http://dataconverter.ti.com">dataconverter.ti.com</a>
DLP® Products	<a href="http://www.dlp.com">www.dlp.com</a>
DSP	<a href="http://dsp.ti.com">dsp.ti.com</a>
Clocks and Timers	<a href="http://www.ti.com/clocks">www.ti.com/clocks</a>
Interface	<a href="http://interface.ti.com">interface.ti.com</a>
Logic	<a href="http://logic.ti.com">logic.ti.com</a>
Power Mgmt	<a href="http://power.ti.com">power.ti.com</a>
Microcontrollers	<a href="http://microcontroller.ti.com">microcontroller.ti.com</a>
RFID	<a href="http://www.ti-rfid.com">www.ti-rfid.com</a>
OMAP Applications Processors	<a href="http://www.ti.com/omap">www.ti.com/omap</a>
Wireless Connectivity	<a href="http://www.ti.com/wirelessconnectivity">www.ti.com/wirelessconnectivity</a>

### Applications

Automotive and Transportation	<a href="http://www.ti.com/automotive">www.ti.com/automotive</a>
Communications and Telecom	<a href="http://www.ti.com/communications">www.ti.com/communications</a>
Computers and Peripherals	<a href="http://www.ti.com/computers">www.ti.com/computers</a>
Consumer Electronics	<a href="http://www.ti.com/consumer-apps">www.ti.com/consumer-apps</a>
Energy and Lighting	<a href="http://www.ti.com/energy">www.ti.com/energy</a>
Industrial	<a href="http://www.ti.com/industrial">www.ti.com/industrial</a>
Medical	<a href="http://www.ti.com/medical">www.ti.com/medical</a>
Security	<a href="http://www.ti.com/security">www.ti.com/security</a>
Space, Avionics and Defense	<a href="http://www.ti.com/space-avionics-defense">www.ti.com/space-avionics-defense</a>
Video and Imaging	<a href="http://www.ti.com/video">www.ti.com/video</a>

### TI E2E Community

[e2e.ti.com](http://e2e.ti.com)