DATA SHEET

TDA9901
Wideband differential digital controlled variable gain amplifier

Objective specification
File under Integrated Circuits, IC02

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Philips
Semiconductors

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Wideband differential digital controlled variable gain amplifier

TDA9901

FEATURES

- 125 MHz, –3 dB bandwidth
- Digitally controlled gain
- TTL/CMOS compatible digital inputs (3 or 5 V)
- Differential clock input; PECL compatible
- 24 dB gain control range
- Five steps of 6 dB plus 6 dB fixed gain
- 30 dB gain maximum
- High impedance differential inputs
- Low impedance differential outputs
- High power supply rejection
- 160 nV/√Hz output voltage noise density at 30 dB gain
- Fast gain settling
- Dual control modes: transparent or latched.

APPLICATIONS

- Linear AGC systems
- IF amplifier in IF conversion systems (e.g. base stations or satellite receivers)
- Instrumentation
- Multi-purpose amplifier
- Driver for differential ADCs (e.g. TDA8768).

GENERAL DESCRIPTION

The TDA9901 is a wideband, low noise amplifier with differential inputs and outputs. The TDA9901 incorporates an AGC function with digital control. The TDA9901 is optimized for fast between different gain settings, preserving small phase and amplitude error.

The TDA9901 presents an excellent combination of low noise and good linearity for a wide input frequency range.

The TDA9901 is optimized for processing IF signals in GSM base stations. It is also suited for many other applications as a general purpose digitally controlled variable gain amplifier.

The TDA9901 is able to operate from a 5 V supply for the analog part and from 2.7 to 5.25 V for the digital part.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{DDA}	analog supply voltage		4.75	5.0	5.25	V
V_{DDD}	digital supply voltage		3.0	3.3	5.25	V
I_{DDA}	analog supply current			31		mA
I_{DDD}	digital supply current			1		mA
G_{diff}	differential gain	minimum gain	–	6	7	dB
		maximum gain	29	30	–	dB
B_{-3dB}	–3 dB bandwidth		125	150	–	MHz
P_{tot}	total power consumption		–	150	200	mW

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
TDA9901TS	SSOP20	plastic shrink small outline package; 20 leads; body width 4.4 mm	SOT266-1

BLOCK DIAGRAM

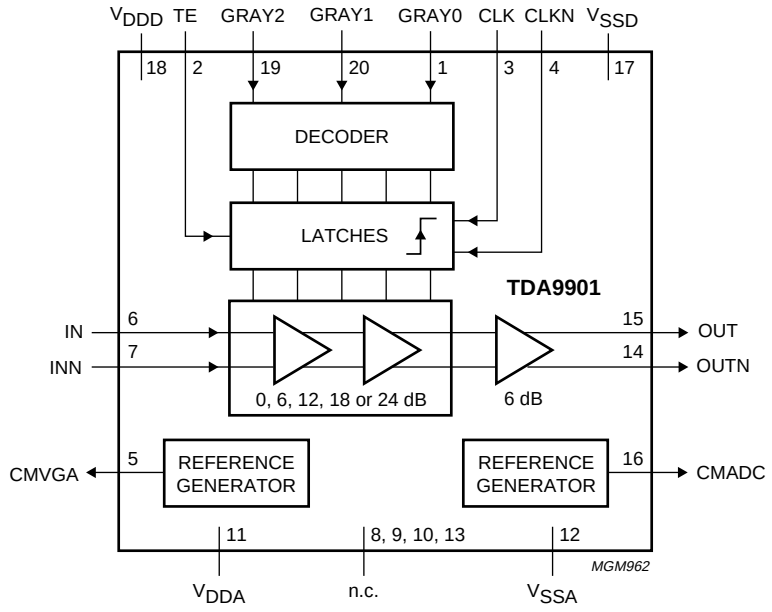


Fig.1 Block diagram.

PINNING

SYMBOL	PIN	DESCRIPTION
GRAY0	1	digital control signal bit 0 input (LSB)
TE	2	transparent enable input
CLK	3	clock input for gain control setting
CLKN	4	inverting clock input for gain control setting
CMVGA	5	regulator output common mode VGA input
IN	6	non-inverting analog input
INN	7	inverting analog input
n.c.	8	not connected
n.c.	9	not connected
n.c.	10	not connected
V_{DDA}	11	analog supply voltage
V_{SSA}	12	analog ground
n.c.	13	not connected
OUTN	14	inverting analog output
OUT	15	non-inverting analog output
CMADC	16	regulator output common mode ADC input
V_{SSD}	17	digital ground
V_{DDD}	18	digital supply voltage
GRAY2	19	digital control signal bit 2 input (MSB)
GRAY1	20	digital control signal bit 1 input

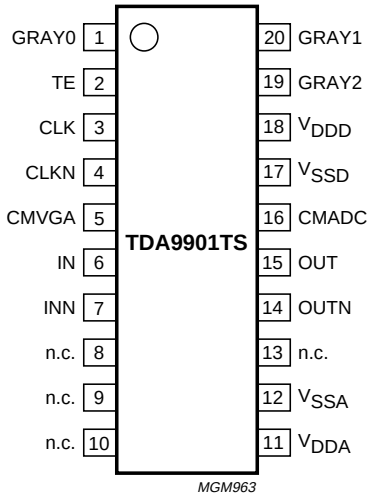


Fig.2 Pin configuration.

FUNCTIONAL DESCRIPTION

The TDA9901 provides a digitally controlled variable gain function for high-frequency applications.

The TDA9901 can be operated in two different modes, depending on the value at pin TE. When TE is at logic 1, the gain can be instantly controlled when the clock signal is HIGH (transparent mode). The gain is fixed during the LOW period of the clock. When TE is at logic 0 the gain of the TDA9901 is changed at the rising edge of the clock signal.

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_{DDA}	analog supply voltage	–0.3	+7.0	V
V_{DDD}	digital supply voltage	–0.3	+7.0	V
ΔV_{DD}	supply voltage difference between V_{DDA} and V_{DDD}	–1.0	+4.0	V
V_I	input voltage level	–0.3	+7.0	V
I_O	output current	–	+10	mA
T_{stg}	storage temperature	–55	+150	°C
T_{amb}	operating ambient temperature	–10	+85	°C
T_j	junction temperature	–	+150	°C

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	VALUE	UNIT
$R_{th(j-a)}$	thermal resistance from junction to ambient in free air	120	K/W

HANDLING

Inputs and outputs are protected against electrostatic discharges in normal handling. However, to be totally safe, it is desirable to take normal precautions appropriate to handling integrated circuits.

CHARACTERISTICS

$V_{DDA} = V_{11}$ to V_{12} = 4.75 to 5.25 V; $V_{DDD} = V_{18}$ to V_{17} = 3.0 to 5.25 V; V_{SSA} and V_{SSD} shorted together; T_{amb} = –10 to + 85 °C; typical values measured at V_{DDA} = 5.0 V; V_{DDD} = 3.3 V and T_{amb} = 25 °C; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supplies						
V_{DDA}	analog supply voltage		4.75	5.0	5.25	V
V_{DDD}	digital supply voltage		3.0	3.3	5.25	V
ΔV_{DD}	voltage difference between V_{CCA} and V_{CCD}		–0.2	–	+2.5	V
I_{DDA}	analog supply current		–	31	–	mA
I_{DDD}	digital supply current		–	1	–	mA
Variable gain amplifier transfer characteristics						
B_{-3dB}	– dB bandwidth	T_{amb} = 25 °C	125	150	–	MHz
$t_{d(g)}$	group delay time	up to f_i = 20 MHz; T_{amb} = 25 °C				
		minimum gain	-	1.35	-	ps
		maximum gain	-	1.35	-	ps
$\Delta t_{d(g)}$	group delay difference	6 dB gain step; T_{amb} = 25 °C	–	–	150	ps

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
t_{set}	settling time	10 to 90% maximum output transition; $C_{L(max)}$ = 5 pF on each output; T_{amb} = 25 °C	–	–	2.8	ns
G_{step}	gain step size	DC input	tbf	6	tbf	dB
$G_{(min)}$	minimum gain setting	DC input	tbf	6	7	dB
$G_{(max)}$	maximum gain setting	DC input	29	30	tbf	dB
G_{flat}	gain flatness	DC to 20 MHz; T_{amb} = 25 °C	–	tbf	–	dB
$\Delta G/\Delta T$	gain stability as a function of temperature	G = 6 dB	–	–	tbf	dB/°C
$\Delta G/\Delta V_{DD}$	gain stability as a function of power supply	G = 6 dB	–	–	tbf	dB/V
$\Delta V_{i(os)}$	input offset voltage difference	6 dB gain step	–	tbf	–	mV
F	noise figure	R_S = 50 Ω; f_i = 20 MHz; T_{amb} = 25 °C	–	tbf	–	dB
$V_{n(o)(equi)}$	equivalent output noise voltage spectral density	R_S = 50 Ω; f_i = 20 MHz; T_{amb} = 25 °C				
		G = 6 dB	–	50	–	nV/√Hz
		G =12 dB	–	70	–	nV/√Hz
		G =18 dB	–	90	–	nV/√Hz
		G = 24 dB	–	120	–	nV/√Hz
		G = 30 dB	–	160	–	nV/√Hz
PSSR	power supply reflection ratio	DC to 150 MHz; T_{amb} = 25 °C	–	tbf	–	dB
CMRR	common mode reflection ratio	DC to 150 MHz; T_{amb} = 25 °C	–	tbf	–	dB
Analog inputs						
$V_{i(max)}$	maximum input voltage (peak-to-peak value)	maximum gain	tbf	1.0	–	V
		minimum gain	tbf	31.25	–	mV
$V_{i(cm)}$	common mode input voltage	referenced to V_{DDA}	tbf	2.4	tbf	V
R_i	input resistance		10	–	–	kΩ
C_i	input capacitance		–	–	5	pF
Analog outputs						
$V_{o(max)}$	maximum differential output voltage (peak-to-peak value)	maximum gain	tbf	–	–	V
		minimum gain	tbf	–	–	V
$V_{o(cm)}$	common mode output voltage		–	3.5	–	V
R_o	output resistance		–	10	–	Ω
C_o	output capacitance		–	3	–	pF

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Variable gain amplifier dynamic performance; T_{amb} = 25 °C						
HD_2	2nd harmonic distortion	$V_o = V_{o(max)}$				
		f_o = 1 MHz	–	–71	tbf	dB
		f_o = 5 MHz	–	–70	tbf	dB
		f_o = 10 MHz	–	–62	tbf	dB
		f_o = 20 MHz	–	–56	tbf	dB
HD_3	3rd harmonic distortion	$V_o = V_{o(max)}$				
		f_o = 1 MHz	–	–51	tbf	dB
		f_o = 5 MHz	–	–51	tbf	dB
		f_o = 10 MHz	–	–50	tbf	dB
		f_o = 20 MHz	–	–48	tbf	dB
Reference voltage output ADC (pin CMADC)						
$V_{ref(CMADC)}$	ADC reference output voltage	referenced to V_{DDA}	tbf	3.5	tbf	V
$R_{o(CMADC)}$	output resistance		–	50	–	Ω
$C_{o(CMADC)}$	output capacitance		–	3	–	pF
Reference voltage output VGA (pin CMVGA)						
$V_{ref(CMVGA)}$	VGA reference output voltage	referenced to V_{DDA}	tbf	2.4	tbf	V
$R_{o(CMVGA)}$	output resistance		–	50	–	Ω
$C_{o(CMVGA)}$	output capacitance		–	3	–	pF
Gain switching characteristics (in latched mode); f_{CLK} = 50 MHz; T_{amb} = 25 °C						
t_h	input data hold time		tbf	0.5	–	ns
t_{su}	input data set-up time		–	2.1	tbf	ns
t_{pd1}	propagation delay time		–	4.25	tbf	ns
t_{set1}	gain settling time	10 to 90% full scale if ±6 dB gain change	–	5.9	tbf	ns
Gain switching characteristics (in transparent mode); f_{CLK} = 50 MHz; T_{amb} = 25 °C						
t_{pd2}	propagation delay time		–	5.0	tbf	ns
t_{set2}	gain settling time	10 to 90% full scale if ±16 dB gain change	–	5.9	tbf	ns
Clock timing input (pin CLKIN)						
$f_{CLK(max)}$	maximum clock frequency		52	–	–	MHz
t_{CLKL}	clock pulse width LOW		8.5	–	–	ns
t_{CLKH}	clock pulse width HIGH		8.5	–	–	ns
t_r	clock rise time		–	4	–	ns
t_f	clock fall time		–	4	–	ns
Digital inputs: pins TE, GRAY0, GRAY1 and GRAY2						
V_{IL}	LOW-level input voltage		0	–	0.8	V
V_{IH}	HIGH-level input voltage		2.0	–	V_{DDD}	V
I_{IH}	HIGH-level input current		–10	–	+10	μA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I_{IL}	LOW-level input current		–10	–	+10	µA
C_i	input capacitance		–	–	3	pF
Clock inputs						
V_{IL}	LOW-level input voltage	V_{DDA} = 5.0 V; note 5	3.19	–	3.52	V
V_{IH}	HIGH-level input voltage	V_{DDA} = 5.0 V; note 5	3.83	–	4.12	V
I_{IH}	HIGH-level input current		–10	–	–	µA
I_{IL}	LOW-level input current		–	–	10	µA
C_i	input capacitance		–	–	2	pF
ΔV_{CLK}	differential AC input voltage for switching (VCLK to VCLKN) (peak-to-peak value)	DC voltage level = 2.5 V	0.5	–	2.0	V

Notes

1. In latching mode (TE = 0), the gain settling is latched at the rising edge of the clock input.
2. In transparent mode, the gain settling directly controlled by the input data pattern.
3. The analog output voltages are positive with respect to AGND.
4. Due to on-chip regulator behaviour a warm-up time of 1 minute (typ.) is recommended for optimal performance
   a) The circuit has two clock inputs: CLK and CLKN. There are four modes of operation:
   b) PECL mode 1: (DC level vary 1 : 1 with V_{DDA}) CLK and CLKN inputs are differential PECL levels.
   c) PECL mode 2: (DC level vary 1 : 1 with V_{DDA}) CLK input is at PECL level and gain change takes place on the rising edge of the clock input signal when in latched mode. A DC level of 3.65 V has to be applied on CLKN decoupled to V_{SSD} via a 100 nF capacitor.
   d) PECL mode 3: (DC level vary 1 : 1 with V_{DDA}) CLK input is at PECL level and gain change takes place on the rising edge of the clock input signal when in latched mode. A DC level of 3.65 V has to be applied on CLKN decoupled to V_{SSD} via a 100 nF capacitor.
   e) AC driving mode 4: when driving the CLK input directly and with any DC signal of minimum 0.5 V (p-p) and with a DC level of 2.5 V, the gain change takes place on the rising edge of the clock signal. When driving the CLKN input with the same signal, gain change takes place on the falling edge of the clock signal. It is recommended to decoupled the CLKN or CLK input to V_{SSD} via a 100 nF capacitor

Table 1 Input coding

STATE	GREY INPUT DATA CODE			GAIN (dB)
–	D2	D1	D0	–
0	0	0	0	minimum
1	0	0	1	minimum + 6
2	0	1	1	minimum + 12
3	0	1	0	minimum + 18
4	1	1	0	minimum + 24
Other	–	–	–	minimum + 24

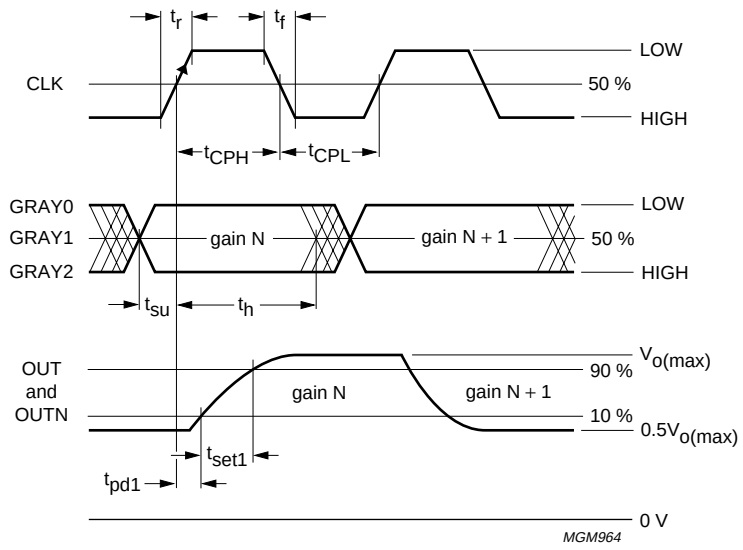


Fig.3 Latched mode timing diagram.

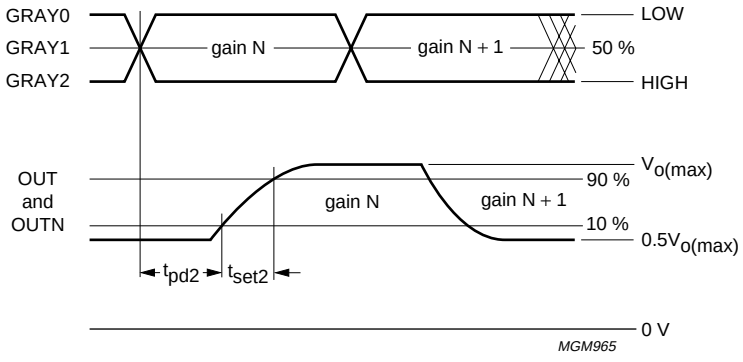
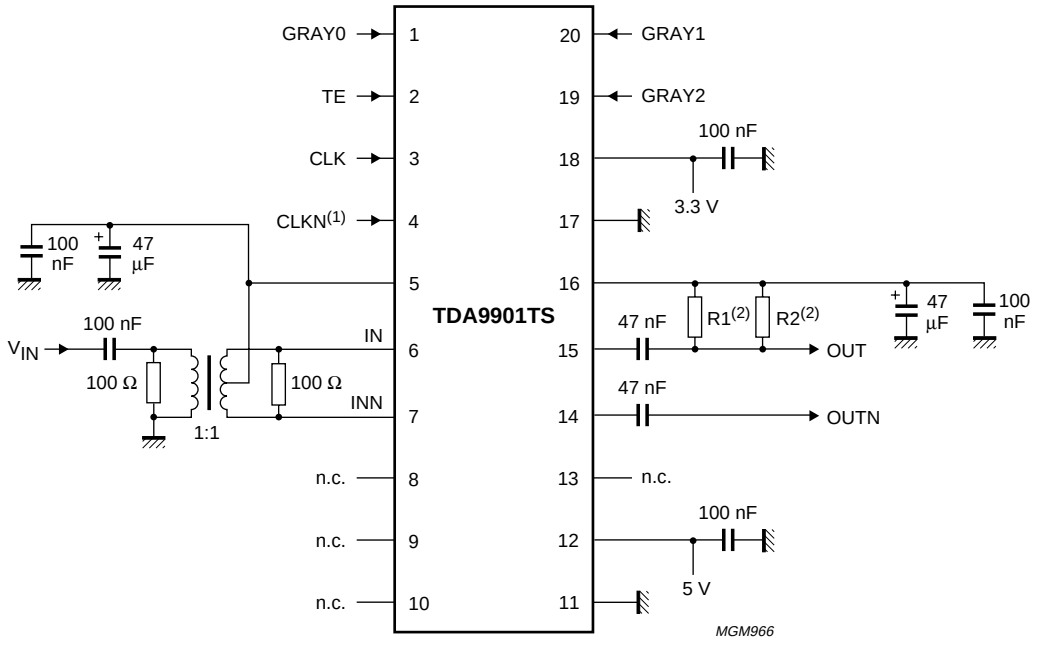


Fig.4 Transparent mode timing diagram with CLK HIGH.

APPLICATION INFORMATION

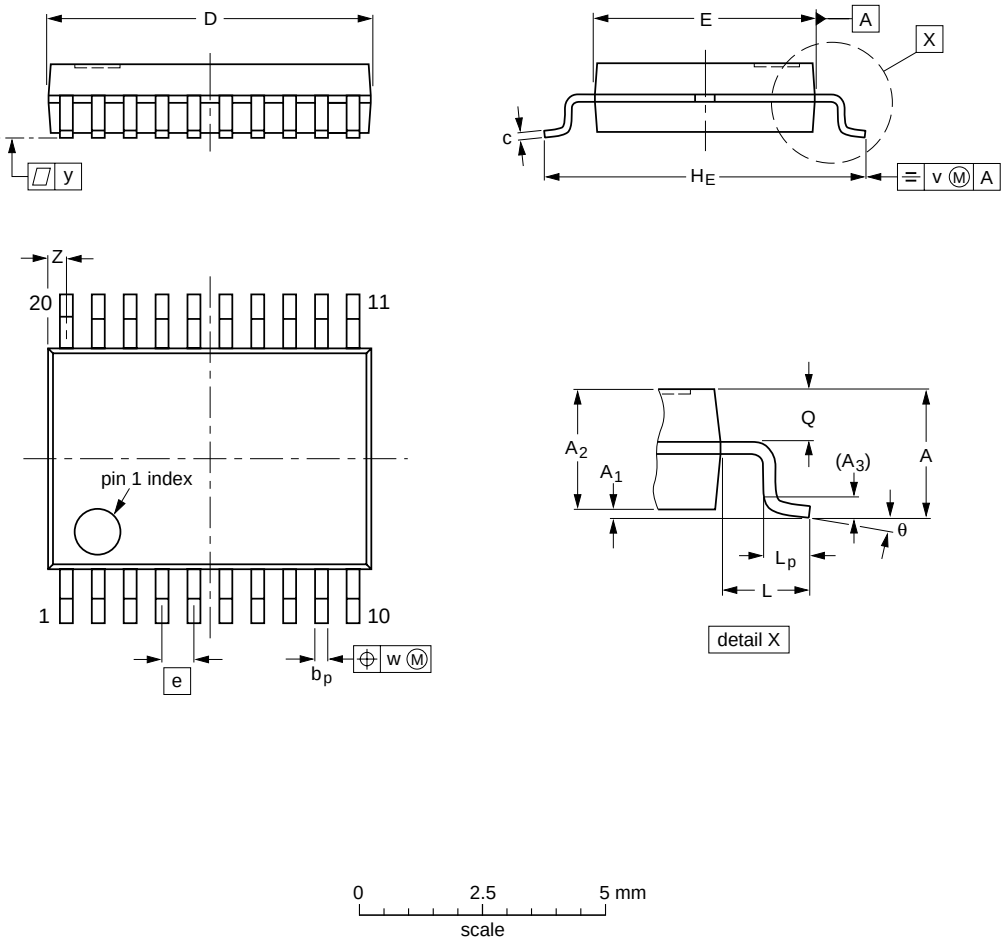


(1) Single-ended clock signal can be applied if required.
(2) R1 and R2 should be at least 680 Ω.

Fig.5 Application diagram.

PACKAGE OUTLINE

SSOP20: plastic shrink small outline package; 20 leads; body width 4.4 mm **SOT266-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_E	L	L_p	Q	v	w	y	$Z^{(1)}$	θ
mm	1.5	0.15 0	1.4 1.2	0.25	0.32 0.20	0.20 0.13	6.6 6.4	4.5 4.3	0.65	6.6 6.2	1.0	0.75 0.45	0.65 0.45	0.2	0.13	0.1	0.48 0.18	10^o 0^o

Note

1. Plastic or metal protrusions of 0.20 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES					EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ				
SOT266-1							~~90-04-05~~ 95-02-25

SOLDERING

Introduction

There is no soldering method that is ideal for all IC packages. Wave soldering is often preferred when through-hole and surface mounted components are mixed on one printed-circuit board. However, wave soldering is not always suitable for surface mounted ICs, or for printed-circuits with high population densities. In these situations reflow soldering is often used.

This text gives a very brief insight to a complex technology. A more in-depth account of soldering ICs can be found in our *"Data Handbook IC26; Integrated Circuit Packages"* (order code 9398 652 90011).

Reflow soldering

Reflow soldering techniques are suitable for all SSOP packages.

Reflow soldering requires solder paste (a suspension of fine solder particles, flux and binding agent) to be applied to the printed-circuit board by screen printing, stencilling or pressure-syringe dispensing before package placement.

Several techniques exist for reflowing; for example, thermal conduction by heated belt. Dwell times vary between 50 and 300 seconds depending on heating method. Typical reflow temperatures range from 215 to 250 °C.

Preheating is necessary to dry the paste and evaporate the binding agent. Preheating duration: 45 minutes at 45 °C.

Wave soldering

Wave soldering is **not** recommended for SSOP packages. This is because of the likelihood of solder bridging due to closely-spaced leads and the possibility of incomplete solder penetration in multi-lead devices.

If wave soldering cannot be avoided, the following conditions must be observed:

- **A double-wave (a turbulent wave with high upward pressure followed by a smooth laminar wave) soldering technique should be used.**
- **The longitudinal axis of the package footprint must be parallel to the solder flow and must incorporate solder thieves at the downstream end.**

Even with these conditions, only consider wave soldering SSOP packages that have a body width of 4.4 mm, that is SSOP16 (SOT369-1) or SSOP20 (SOT266-1).

During placement and before soldering, the package must be fixed with a droplet of adhesive. The adhesive can be applied by screen printing, pin transfer or syringe dispensing. The package can be soldered after the adhesive is cured.

Maximum permissible solder temperature is 260 °C, and maximum duration of package immersion in solder is 10 seconds, if cooled to less than 150 °C within 6 seconds. Typical dwell time is 4 seconds at 250 °C.

A mildly-activated flux will eliminate the need for removal of corrosive residues in most applications.

Repairing soldered joints

Fix the component by first soldering two diagonally-opposite end leads. Use only a low voltage soldering iron (less than 24 V) applied to the flat part of the lead. Contact time must be limited to 10 seconds at up to 300 °C. When using a dedicated tool, all other leads can be soldered in one operation within 2 to 5 seconds between 270 and 320 °C.

DEFINITIONS

Data sheet status	
Objective specification	This data sheet contains target or goal specifications for product development.
Preliminary specification	This data sheet contains preliminary data; supplementary data may be published later.
Product specification	This data sheet contains final product specifications.
Limiting values	
Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.	
Application information	
Where application information is given, it is advisory and does not form part of the specification.	

LIFE SUPPORT APPLICATIONS

These products are not designed for use in life support appliances, devices, or systems where malfunction of these products can reasonably be expected to result in personal injury. Philips customers using or selling these products for use in such applications do so at their own risk and agree to fully indemnify Philips for any damages resulting from such improper use or sale.

NOTES

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