

DATA SHEET

TDA8559

Low-voltage stereo headphone amplifier

Product specification
Supersedes data of 1996 Jan 02
File under Integrated Circuits, IC01

1997 Jun 27

Low-voltage stereo headphone amplifier

TDA8559

FEATURES

- Operating voltage from 1.9 to 30 V
- Very low quiescent current
- Low distortion
- Few external components
- Differential inputs
- Usable as a mono amplifier in Bridge-Tied Load (BTL) or stereo Single-Ended (SE)
- Single-ended mode without loudspeaker capacitor
- Mute and standby mode
- Short-circuit proof to ground, to supply voltage (<10 V) and across load
- No switch on or switch off clicks
- ESD protected on all pins.

APPLICATIONS

- Portable telephones
- Walk-mans
- Portable audio
- Mains fed equipment.

GENERAL DESCRIPTION

The TDA8559 is a stereo amplifier that operates over a wide supply voltage range from 1.9 to 30 V and consumes a very low quiescent current. This makes it suitable for battery fed applications (2×1.5 V cells). Because of an internal voltage buffer, this device can be used with or without a capacitor connected in series with the load. It can be applied as a headphone amplifier, but also as a mono amplifier with a small speaker (25Ω), or as a line driver in mains applications.

QUICK REFERENCE DATA

| SYMBOL | PARAMETER | CONDITIONS | MIN. | TYP. | MAX. | UNIT |
|---------------------------|---------------------------------|-------------------------------|------|-------|------|---------------|
| Supplies | | | | | | |
| V_P | operating supply voltage | | 1.9 | 3 | 30 | V |
| $I_{q(\text{tot})}$ | total quiescent current | | – | 2.75 | 4 | mA |
| I_{stb} | standby supply current | | – | – | 10 | μA |
| Stereo application | | | | | | |
| P_o | output power | THD = 10% | 30 | 35 | – | mW |
| THD | total harmonic distortion | $P_o = 20$ mW; $f_i = 1$ kHz | – | 0.075 | 0.15 | % |
| | | $P_o = 20$ mW; $f_i = 10$ kHz | – | 0.1 | – | % |
| G_v | voltage gain | | 25 | 26 | 27 | dB |
| f_{ss} | small signal roll-off frequency | –1 dB | – | 750 | – | kHz |
| BTL application | | | | | | |
| P_o | output power | THD = 10% | 125 | 140 | – | mW |
| THD | total harmonic distortion | $P_o = 70$ mW; $f_i = 1$ kHz | – | 0.05 | 0.1 | % |
| | | $P_o = 70$ mW; $f_i = 10$ kHz | – | 0.2 | – | % |
| G_v | voltage gain | | 31 | 32 | 33 | dB |

ORDERING INFORMATION

| TYPE NUMBER | PACKAGE | | |
|-------------|---------|---|----------|
| | NAME | DESCRIPTION | VERSION |
| TDA8559 | DIP16 | plastic dual in-line package; 16 leads (300 mil); long body | SOT38-1 |
| TDA8559T | SO16 | plastic small outline package; 16 leads; body width 3.9 mm | SOT109-1 |

Low-voltage stereo headphone amplifier

TDA8559

BLOCK DIAGRAM

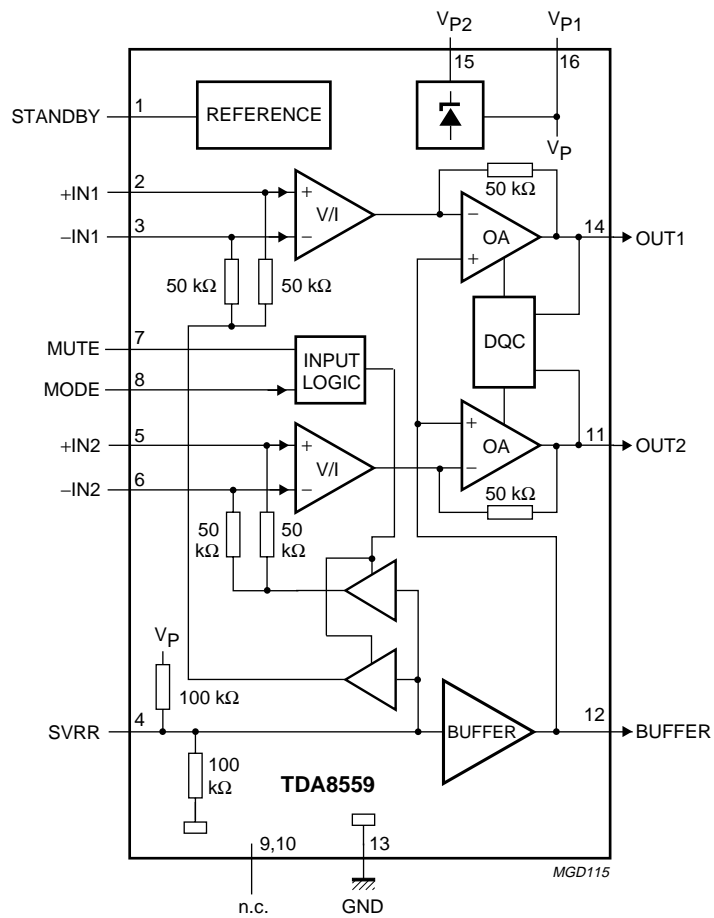


Fig.1 Block diagram.

Low-voltage stereo headphone amplifier

TDA8559

PINNING

| SYMBOL | PIN | DESCRIPTION |
|----------|-----|---------------------------------|
| STANDBY | 1 | standby select |
| +IN1 | 2 | non-inverting input 1 |
| -IN1 | 3 | inverting input 1 |
| SVRR | 4 | supply voltage ripple rejection |
| +IN2 | 5 | non-inverting input 2 |
| -IN2 | 6 | inverting input 2 |
| MUTE | 7 | mute select |
| MODE | 8 | input mode select |
| n.c. | 9 | not connected |
| n.c. | 10 | not connected |
| OUT2 | 11 | output 2 |
| BUFFER | 12 | buffer output ($0.5V_P$) |
| GND | 13 | ground |
| OUT1 | 14 | output 1 |
| V_{P2} | 15 | high supply voltage |
| V_{P1} | 16 | low supply voltage |

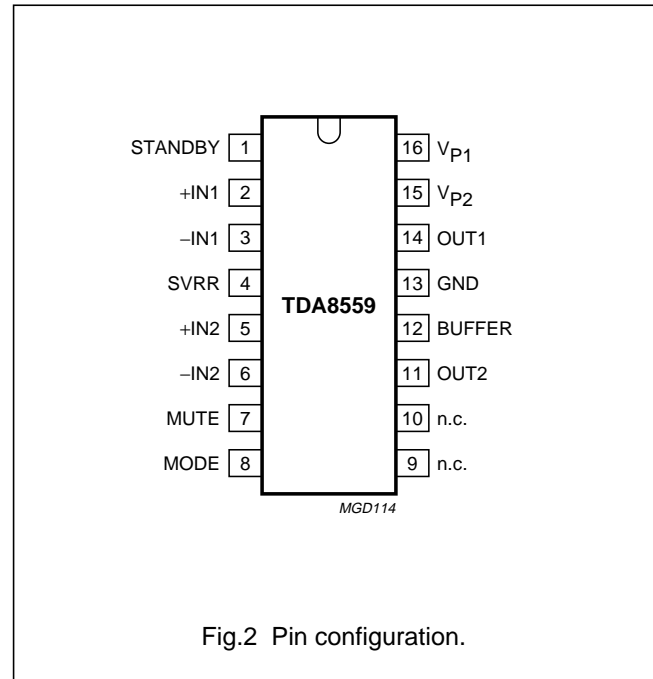


Fig.2 Pin configuration.

FUNCTIONAL DESCRIPTION

The TDA8559 contains two amplifiers with differential inputs, a $0.5V_P$ output buffer and a high supply voltage stabilizer. Each amplifier consists of a voltage-to-current converter (V/I), an output amplifier and a common dynamic quiescent current controller. The gain of each amplifier is internally fixed at 26 dB ($= 20 \times$). The $0.5V_P$ output can be used as a replacement for the single-ended capacitors. The two amplifiers can also be used as a mono amplifier in a BTL configuration thereby resulting in more output power.

With three mode select pins, the device can be switched into the following modes:

1. Standby mode ($I_P < 10 \mu A$)
2. Mute mode
3. Operation mode, with two input selections (the input source is directly connected or connected via coupling capacitors at the input).

The ripple rejection in the stereo application with a single-ended capacitor can be improved by connecting a capacitor between the $0.5V_P$ capacitor pin and ground.

The device is fully protected against short-circuiting of the output pins to ground, to the low supply voltage pin and across the load.

V/I converters

The V/I converters have a transconductance of $400 \mu S$. The inputs are completely symmetrical and the two amplifiers can be used in opposite phase. The mute mode causes the V/I converters to block the input signal. The input mode pin selects two applications in which the V/I converters can be used.

The first application (input mode pin floating) is used with a supply voltage below 6 V. The input DC level is at ground level (the unused input pin connected to ground) and no input coupling capacitors are necessary. The maximum converter output current is sufficient to obtain an output swing of 3 V (peak).

In the second application with a supply voltage greater than 6 V (input mode pin HIGH), the input mode pin is connected to V_P . In this configuration (input DC level = $0.5V_P + 0.6 V$) the input source must be coupled with a capacitor and the two unused input pins must be connected via a capacitor to ground, to improve noise performance. This application has a higher quiescent current, because the maximum output current of the V/I converter is higher to obtain an output voltage swing of 9 V (peak).

Low-voltage stereo headphone amplifier

TDA8559

Output amplifiers

The output amplifiers have a transresistance of 50 k Ω , a bandwidth of approximately 750 kHz and a maximum output current of 100 mA. The mid-tap output voltage equals the voltage applied at the non-inverting pin of the output amplifier. This pin is connected to the output of the 0.5V_P buffer. This reduces the distortion when the load is connected between an output amplifier and the buffer (because feedback is applied over the load).

Buffer

The buffer delivers 0.5V_P to the output with a maximum output (sink and source) current of 200 mA (peak).

Dynamic quiescent controller

The Dynamic Quiescent Current controller (DQC) gives the advantage of low quiescent current and low distortion. When there are high frequencies in the output signal, the DQC will increase the quiescent current of the two output amplifiers and the buffer. This will reduce the cross-over distortion that normally occurs at high frequencies and low quiescent current. The DQC gives output currents that are linear with the amplitude and the frequency of the output signals. These currents control the quiescent current.

Stabilizer

The TDA8559 has a voltage supply range from 1.9 to 30 V. This range is divided over two supply voltage pins. Pin 16 is 1.9 to 18 V (breakdown voltage of the process); this pin is preferred for supply voltages less than 18 V. Pin 15 is used for applications where V_P is approximately 6 to 30 V. The stabilizer output is internally connected to the supply voltage pin 16. In the range from 6 to 18 V, the voltage drop to pin 16 is 1 V. In the range from 18 to 30 V the stabilizer output voltage (to pin 16) is approximately 17 V.

Input logic

The MUTE pin (pin 7) selects the mute mode of the V/I converters. LOW (TTL/CMOS) level is mute. A voltage between 0.5 V (low level) and 1.5 V (high level) causes a soft mute to operate (no plops). When pin 7 is floating or greater than 1.5 V it is in the operating condition.

The input mode pin must be connected to V_P when the supply voltage is greater than 6 V. The input mode logic raises the tail current of the V/I converters and enables the two buffers to bias the inputs of the V/I converters.

Reference

This circuit supplies all currents needed in this device. With the standby mode pin 1 (TTL/CMOS), it is possible to switch to the standby mode and reduce the total quiescent current to below 10 μ A.

Low-voltage stereo headphone amplifier

TDA8559

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

| SYMBOL | PARAMETER | CONDITIONS | MIN. | MAX. | UNIT |
|---------------|---------------------------------|---------------------|------|------|------|
| $V_{P2(max)}$ | maximum supply voltage (pin 15) | | – | 30 | V |
| $V_{P1(max)}$ | maximum supply voltage (pin 16) | | – | 18 | V |
| $V_{i(max)}$ | maximum input voltage | | – | 18 | V |
| I_{ORM} | peak output current | repetitive | – | 150 | mA |
| P_{tot} | total power dissipation | SO16 | – | 1.19 | W |
| | | DIP16 | – | 2.4 | W |
| T_{amb} | operating ambient temperature | | –40 | +85 | °C |
| T_{stg} | storage temperature | | –55 | +150 | °C |
| T_{vj} | virtual junction temperature | | – | 150 | °C |
| t_{sc} | short-circuiting time | $V_P < 10\text{ V}$ | – | 1 | hour |

QUALITY SPECIFICATION

Quality in accordance with "SNW-FQ-611E", if this type is used as an audio amplifier. The number of the quality specification can be found in the "Quality Reference handbook". The handbook can be ordered using the code 9397 750 00192.

THERMAL CHARACTERISTICS

| SYMBOL | DESCRIPTION | VALUE | UNIT |
|---------------|---|-------|------|
| $R_{th\ j-a}$ | thermal resistance from junction to ambient in free air | | |
| | DIP16 | 52 | K/W |
| | SO16 | 105 | K/W |

CHARACTERISTICS

$V_P = 3\text{ V}$; $T_{amb} = 25\text{ °C}$; $f_i = 1\text{ kHz}$; unless otherwise specified.

| SYMBOL | PARAMETER | CONDITIONS | MIN. | TYP. | MAX. | UNIT |
|---------------------------|--------------------------|------------|------|------|------|------|
| DC characteristics | | | | | | |
| V_P | operating supply voltage | note 1 | 1.9 | 3 | 30 | V |
| $I_{q(tot)}$ | total quiescent current | open load | – | 2.75 | 4 | mA |
| I_{stb} | standby supply current | open load | – | – | 10 | μA |
| V_1 | standby mode voltage | standby | 0 | – | 0.5 | V |
| | | operating | 1.5 | – | 18 | V |
| V_7 | mute mode voltage | mute | 0 | – | 0.5 | V |
| | | operating | 1.5 | – | 18 | V |
| I_{bias} | input bias current | | – | 100 | 300 | nA |

Low-voltage stereo headphone amplifier

TDA8559

| SYMBOL | PARAMETER | CONDITIONS | MIN. | TYP. | MAX. | UNIT |
|--|---------------------------------|---|------|-------|------|------------------|
| Single-ended stereo application ($R_L = 32 \Omega$) | | | | | | |
| P_o | output power | THD = 10% | 30 | 35 | – | mW |
| THD | total harmonic distortion | $P_o = 20 \text{ mW}; f_i = 1 \text{ kHz}; \text{ note 2}$ | – | 0.075 | 0.15 | % |
| | | $P_o = 20 \text{ mW}; f_i = 10 \text{ kHz}; \text{ note 2}$ | – | 0.1 | – | % |
| G_v | voltage gain | | 25 | 26 | 27 | dB |
| f_{ss} | small signal roll-off frequency | –1 dB | – | 750 | – | kHz |
| α_{cs} | channel separation | $R_s = 5 \text{ k}\Omega$ | 40 | – | – | dB |
| $ \Delta G_v $ | channel unbalance | | – | – | 1 | dB |
| V_{no} | noise output voltage | note 3 | – | 70 | 85 | μV |
| $V_{no(mute)}$ | noise output voltage in mute | note 3 | – | 20 | 30 | μV |
| $V_{o(mute)}$ | output voltage in mute | note 4 | – | – | 30 | μV |
| V_{mt} | mid-tap voltage | | 1.4 | 1.5 | 1.6 | V |
| Z_i | input impedance | | 75 | 100 | 125 | $\text{k}\Omega$ |
| V_{os} | DC output offset voltage | note 5 | – | – | 100 | mV |
| SVRR | supply voltage ripple rejection | note 6 | 45 | 55 | – | dB |
| BTL application ($R_L = 25 \Omega$) | | | | | | |
| P_o | output power | THD = 10% | 125 | 140 | – | mW |
| THD | total harmonic distortion | $P_o = 70 \text{ mW}; f_i = 1 \text{ kHz}; \text{ note}$ | – | 0.05 | 0.1 | % |
| | | $P_o = 70 \text{ mW}; f_i = 10 \text{ kHz}; \text{ note 2}$ | – | 0.1 | – | % |
| G_v | voltage gain | | 31 | 32 | 33 | dB |
| f_{ss} | small signal roll-off frequency | –1 dB | – | 750 | – | kHz |
| V_{no} | noise output voltage | note 3 | – | 100 | 120 | μV |
| $V_{no(mute)}$ | noise output voltage in mute | note 3 | – | 25 | 40 | μV |
| $V_{o(mute)}$ | output voltage in mute | note 4 | – | – | 40 | μV |
| V_{os} | DC output offset voltage | note 7 | – | – | 150 | mv |
| SVRR | supply voltage ripple rejection | note 6 | 39 | 49 | – | dB |
| Z_i | input impedance | | 39 | 50 | 61 | $\text{k}\Omega$ |
| Line driver application ($R_L \geq 1 \text{ k}\Omega$) | | | | | | |
| V_o | line output voltage | | 0.1 | – | 2.9 | V |

Notes

1. The supply voltage range at pin V_{P1} is from 1.9 to 18 V. Pin V_{P2} is used for the voltage range from 6 to 30 V.
2. Measured with low-pass filter 30 kHz.
3. Noise output voltage measured with a bandwidth of 20 Hz to 20 kHz, unweighted. $R_s = 5 \text{ k}\Omega$.
4. RMS output voltage in mute is measured with $V_i = 200 \text{ mV}$ (RMS); $f = 1 \text{ kHz}$.
5. DC output offset voltage is measured between the signal output and the $0.5V_P$ output.
6. The ripple rejection is measured with a ripple voltage of 200 mV (RMS) applied to the positive supply rail ($R_s = 0 \text{ k}\Omega$).
7. DC output offset voltage is measured between the two signal outputs.

Low-voltage stereo headphone amplifier

TDA8559

APPLICATION INFORMATION

General

For applications with a maximum supply voltage of 6 V (input mode LOW) the input pins need a DC path to ground (see Figs 3 and 4). For applications with supply voltages in the range from 6 to 18 V (input mode HIGH) the input DC level is $0.5V_P + 0.6$ V. In this situation the input configurations illustrated in Figs 5 and 6 have to be used.

The capacitor C_b is recommended for stability improvement. The value may vary between 10 and 100 nF. This capacitor should be placed close to the IC between pin 12 and pin 13.

Heatsink design

The standard application is stereo headphone single-ended with a 32Ω load impedance to buffer (see Fig.9). The headphone amplifier can deliver a peak output current of 150 mA into the load.

For the DIP16 envelope $R_{th\ j-amb} = 52$ K/W; the maximum sine wave power dissipation for $T_{amb} = 25$ °C is:

$$2.4\ W = \frac{150 - 25}{52}$$

For $T_{amb} = 60$ °C the maximum total power dissipation is:

$$1.7\ W = \frac{150 - 60}{52}$$

For the SO16 envelope $R_{th\ j-amb} = 105$ K/W; the maximum sinewave power dissipation for $T_{amb} = 25$ °C is:

$$1.2\ W = \frac{150 - 25}{105}$$

For $T_{amb} = 60$ °C the maximum total power dissipation is:

$$0.85\ W = \frac{150 - 60}{105}$$

Test conditions

$T_{amb} = 25$ °C; unless otherwise specified: $V_P = 3$ V, $f = 1$ kHz, $R_L = 32 \Omega$, Gain = 26 dB, low input mode, band-pass filter: 22 Hz to 30 kHz. The total harmonic distortion as a function of frequency was measured with low-pass filter of 80 kHz. The quiescent current has been measured without any load impedance.

In applications with coupling capacitors towards the load, an electrolytic capacitor has to be connected to pin 4 (SVRR).

- The graphs for the single-ended application have been measured with the application illustrated in Fig.9; input configuration for input mode low (Fig.4) and input configuration for input mode high (Fig.6).
- The graphs for the BTL application 'input mode low' have been measured with the application circuit illustrated in Fig.11 and the input configuration illustrated in Fig.4.
- The graphs for the line-driver application have been measured with the application circuit illustrated in Fig.13 and the input configuration illustrated in Fig.6; input mode high.

Input configurations

The IC can be applied in two ways, 'input mode low' and 'input mode high'. This can be selected by the input mode at pin 8:

1. Input mode low: pin 8 floating:
The DC level of the input pins has to be between 0 V and ($V_P - 1.8$ V). A DC path to ground is needed. The maximum output voltage is approximately 2.1 V (RMS). Input configurations illustrated in Figs 3 and 4 should be used.
2. Input mode high: pin 8 is connected to V_P :
This mode is intended for supply voltages >6 V. It can deliver a maximum output voltage of approximately 6 V (RMS) at THD = 0.5%. The DC voltage level of the input pins is ($0.5V_P + 0.6$ V). Coupling capacitors are necessary. Input configurations illustrated in Figs 5 and 6 should be used.

Low-voltage stereo headphone amplifier

TDA8559

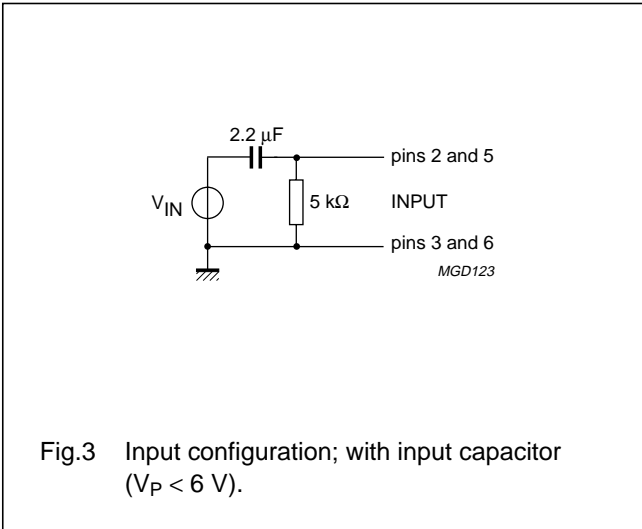


Fig. 3 Input configuration; with input capacitor ($V_P < 6\text{ V}$).

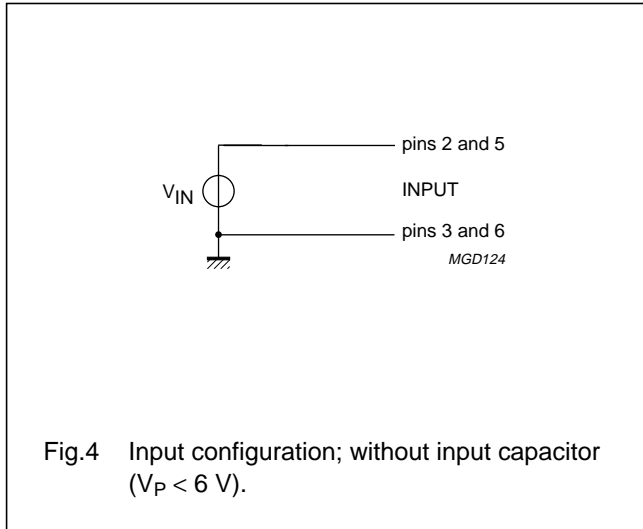


Fig. 4 Input configuration; without input capacitor ($V_P < 6\text{ V}$).

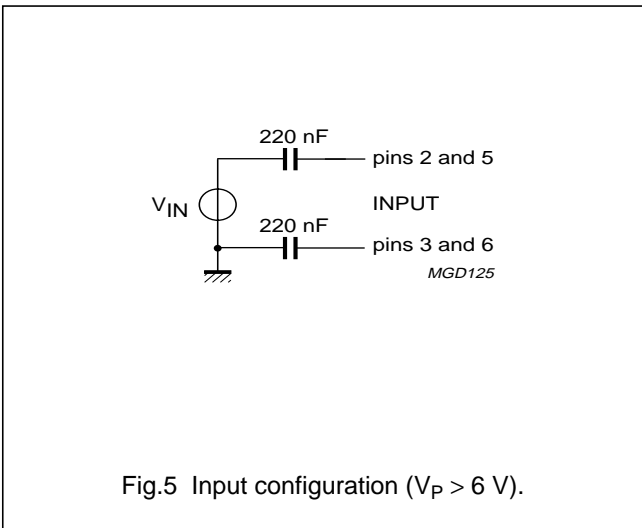


Fig. 5 Input configuration ($V_P > 6\text{ V}$).

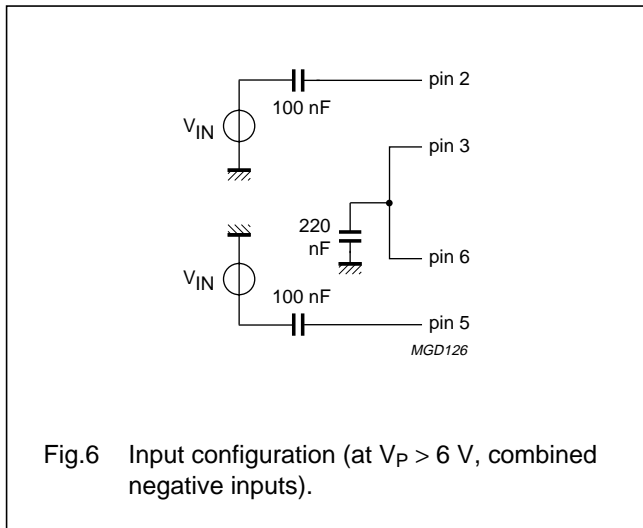


Fig. 6 Input configuration (at $V_P > 6\text{ V}$, combined negative inputs).

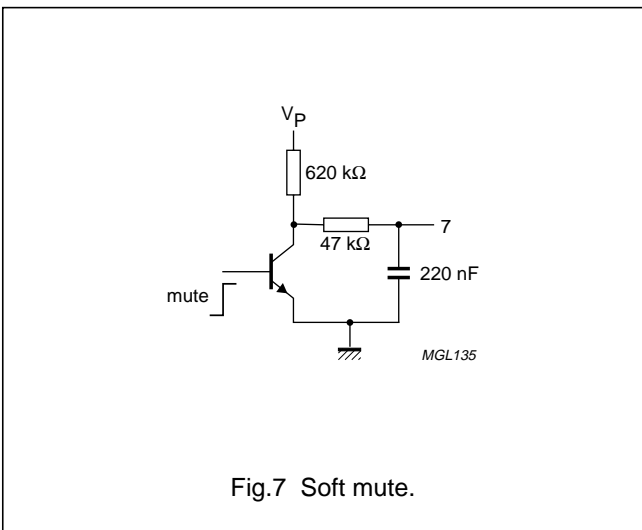


Fig. 7 Soft mute.

Standby/mute

- The standby mode ($V_1 < 0.5\text{ V}$) is intended for power saving purpose. Then the total quiescent current is $< 10\text{ }\mu\text{A}$.
- To avoid 'pop-noise' during switch-on or switch-off the IC can be muted ($V_7 < 0.5\text{ V}$). This can be achieved by a 'soft-mute' circuit or by direct control from a microcontroller.

Low-voltage stereo headphone amplifier

TDA8559

Application 1: SE with loudspeaker capacitor (see Fig.8)

The value of capacitor C_r influences the behaviour of the Supply Voltage Ripple Rejection (SVRR) at low frequencies; increasing the value of C_r increases the performance of the SVRR.

Application 2: SE to buffer (without loudspeaker capacitor) (see Fig.9)

This is the basic headphone application. The advantage of this application with respect to application 1, is that it needs only one external component (C_b) in the event of stability problems.

Application 3: Improved SE to buffer (without loudspeaker capacitor) (see Fig.10)

This application is an improved configuration of application 2. The distinction between the two is connecting the loads in opposite phase. This lowers the average current through the SE buffer.

It should be noted that a headphone cannot be used because the load requires floating terminals.

Application 4: Bridge tied load mono amplifier (see Fig.11)

This configuration delivers four times the output power of the SE application with the same supply and load conditions. The capacitor C_r is not required.

Application 5: Line driver application $1.9\text{ V} < V_P < 6\text{ V}$ (see Fig.12)

The TDA8559 delivers a virtual rail-to-rail output voltage and is also usable in a low voltage environment, as a line driver. In this application the input needs a DC path to ground, input configurations illustrated in Figs 3 and 4 should be used. The value of capacitor C_r influences the behaviour of the SVRR at low frequencies; increasing the value of C_r increases the performance of the SVRR.

Application 6: Line driver application $6\text{ V} < V_P < 18\text{ V}$ (see Fig.13)

The TDA8559T delivers a virtual rail-to-rail output voltage. Because the input mode has to be high, the input configurations illustrated in Figs 5 and 6 should be used. This application can also be used for headphone application, however, due to the limited output current and the limited output power at the headphone, series resistors have to be used between the output pins and the load.

The value of capacitor C_r influences the behaviour of the SVRR at low frequencies; increasing the value of C_r increases the performance of the SVRR.

Application 7: Line driver application $6\text{ V} < V_P < 30\text{ V}$ (see Fig.14)

With the supply voltage connected to pin 15 it is possible to use the head amplifier above the maximum of 18 V to pin 16. The internal supply voltage will be reduced to a maximum of approximately 17 V.

This will be convenient in applications where the supply voltage is higher than 18 V, however an output voltage swing that reaches the higher supply voltage is not required. The input configurations illustrated in Figs 5 and 6 should be used. This application can also be used for headphone applications. However, due to the limited output current, series resistors have to be used between the output pins and the load.

Low-voltage stereo headphone amplifier

TDA8559

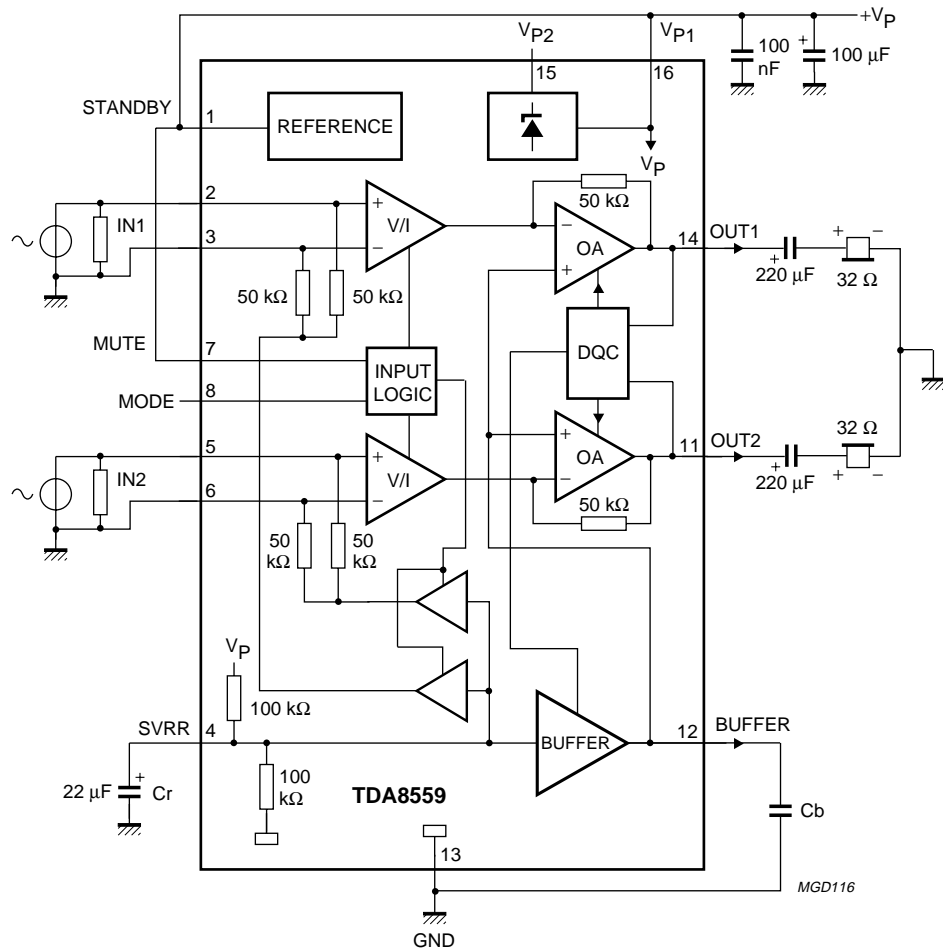


Fig.8 Application 1: single-ended with loudspeaker capacitor.

Low-voltage stereo headphone amplifier

TDA8559

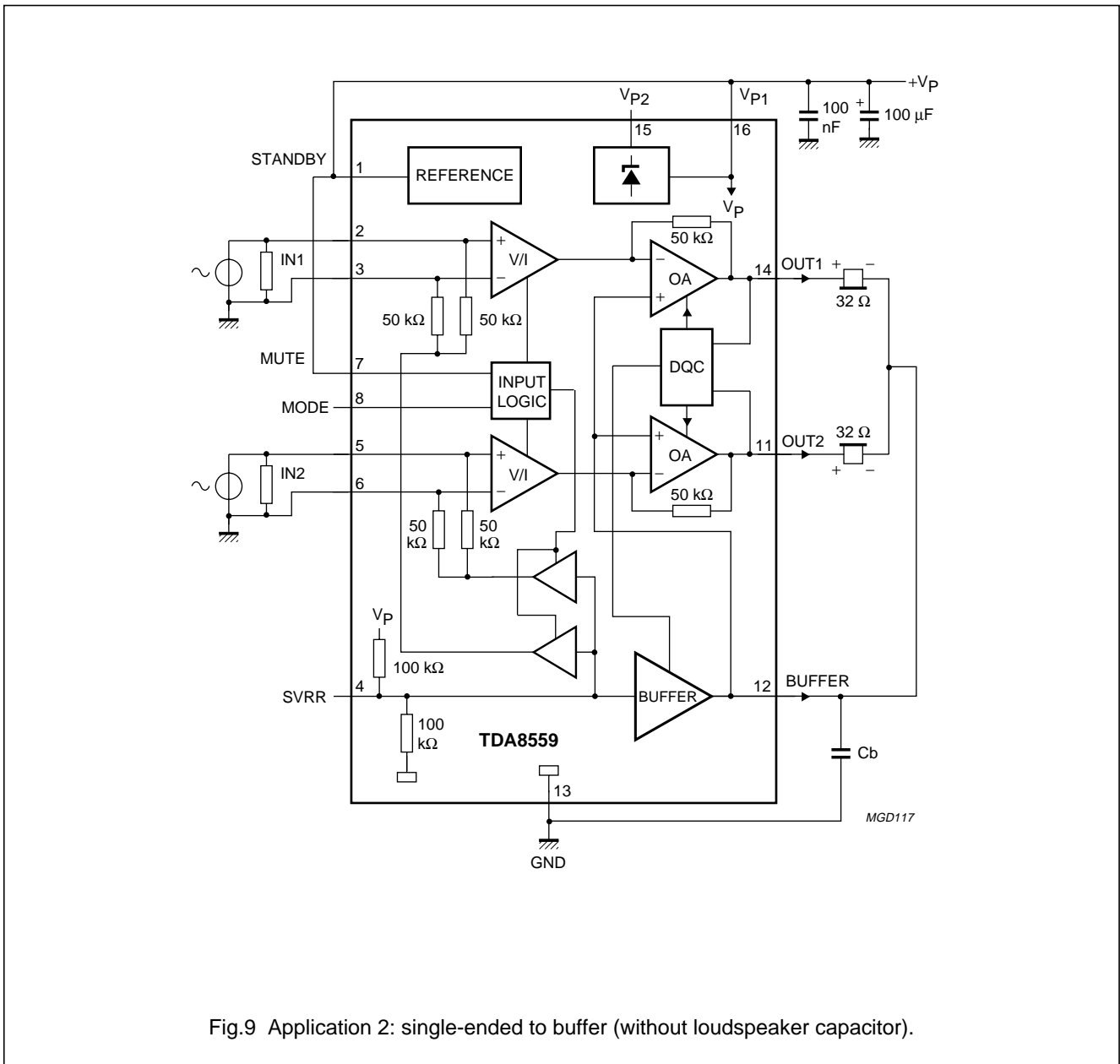


Fig.9 Application 2: single-ended to buffer (without loudspeaker capacitor).

Low-voltage stereo headphone amplifier

TDA8559

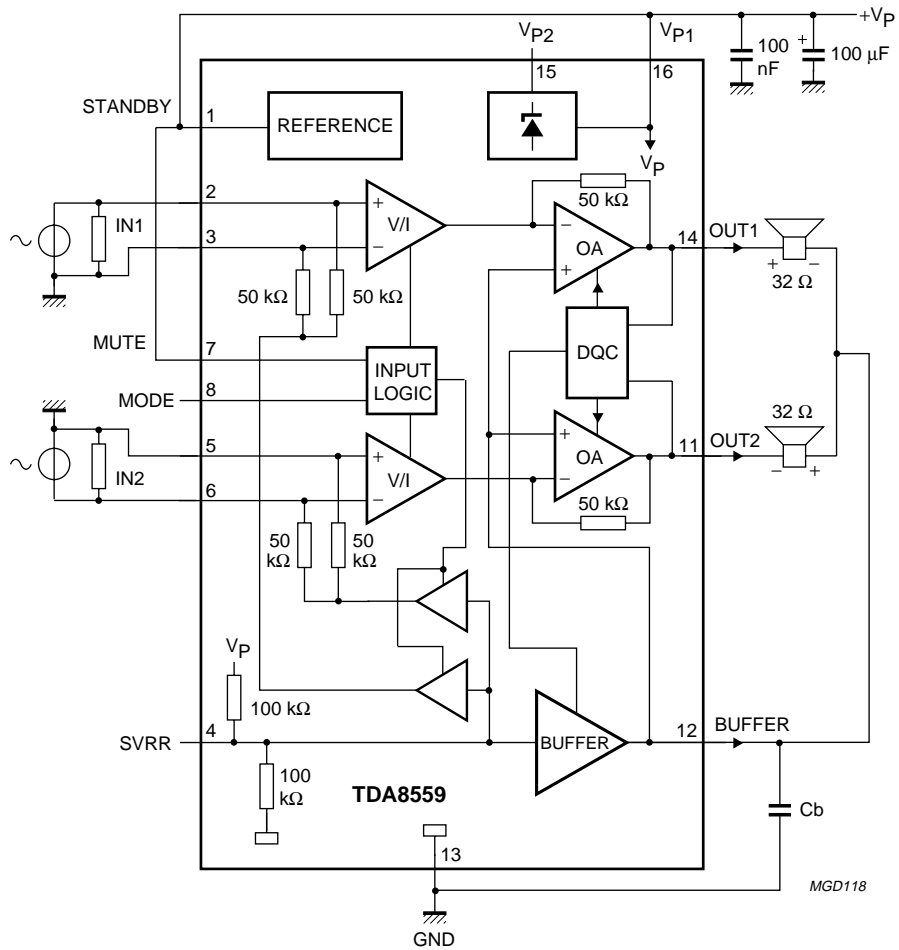


Fig.10 Application 3: Improved single-ended to buffer (without loudspeaker capacitor).

Low-voltage stereo headphone amplifier

TDA8559

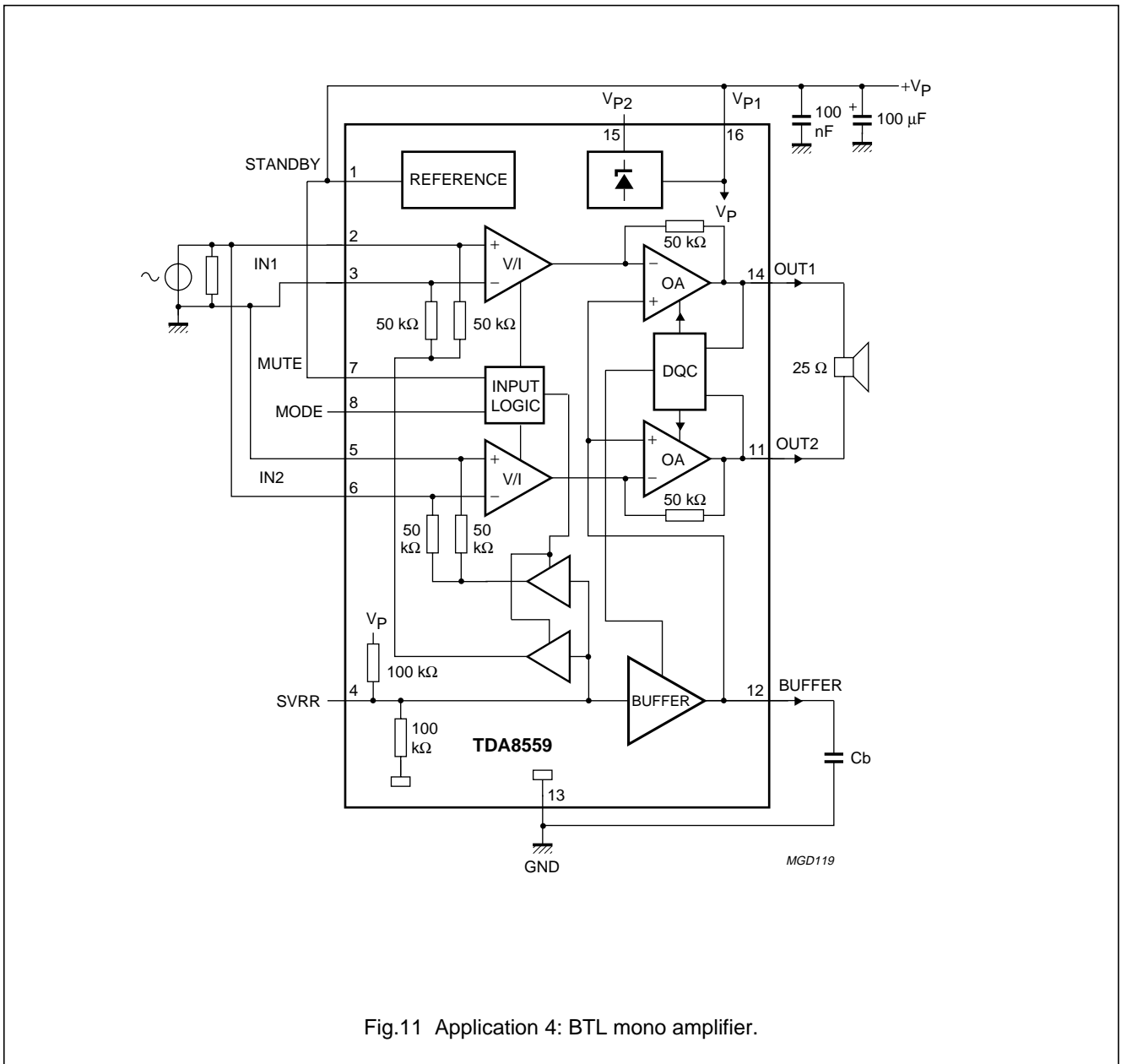


Fig.11 Application 4: BTL mono amplifier.

Low-voltage stereo headphone amplifier

TDA8559

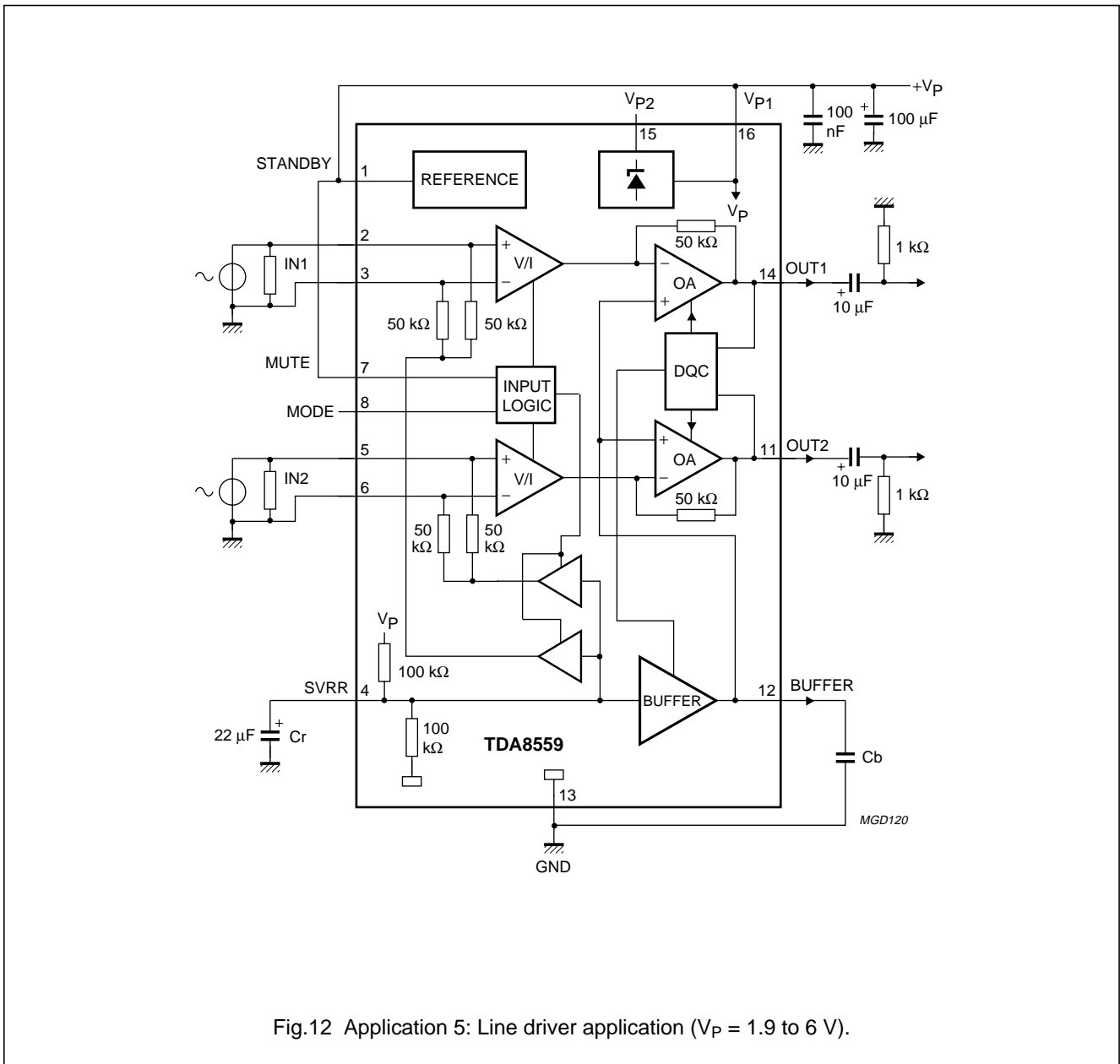


Fig.12 Application 5: Line driver application ($V_P = 1.9$ to 6 V).

Low-voltage stereo headphone amplifier

TDA8559

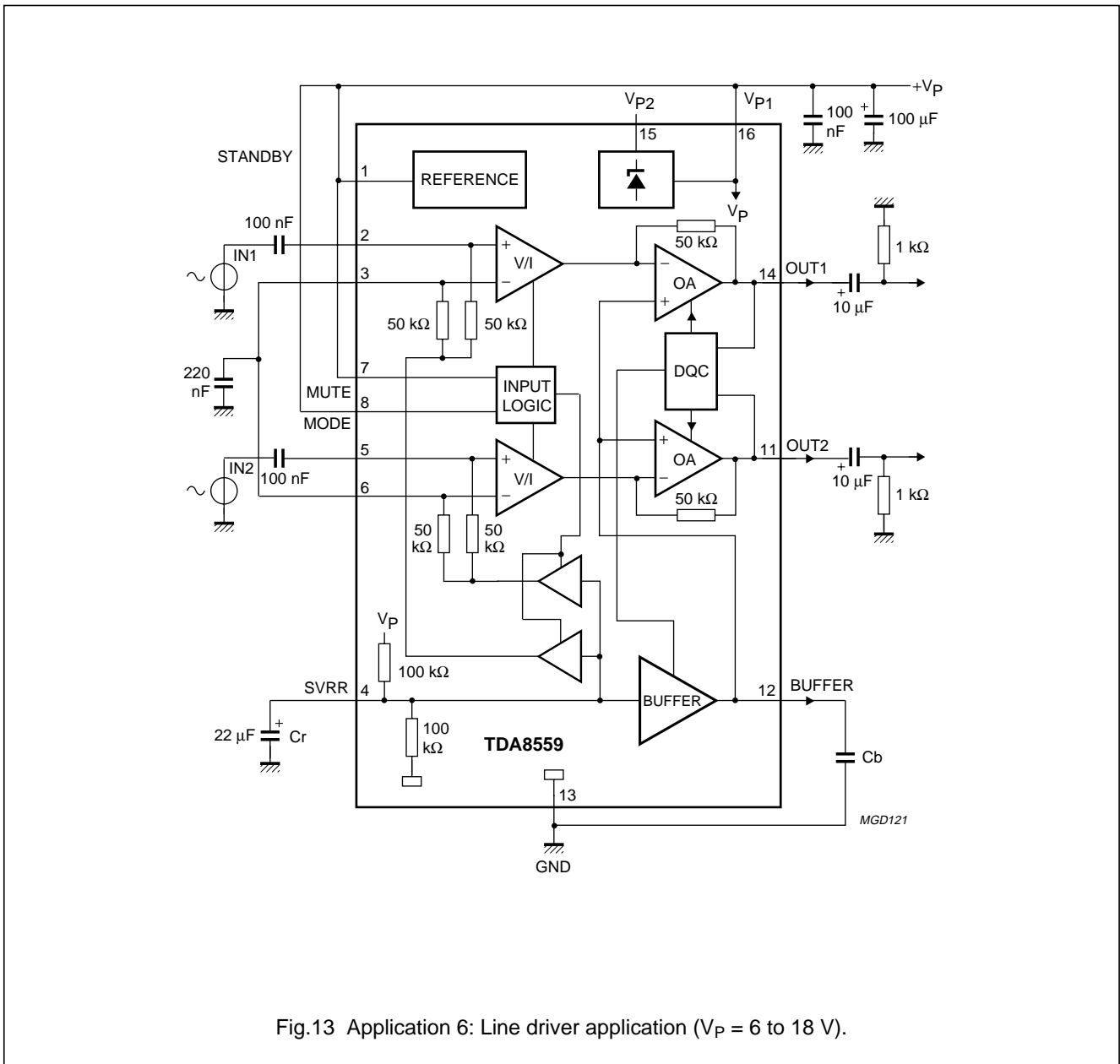
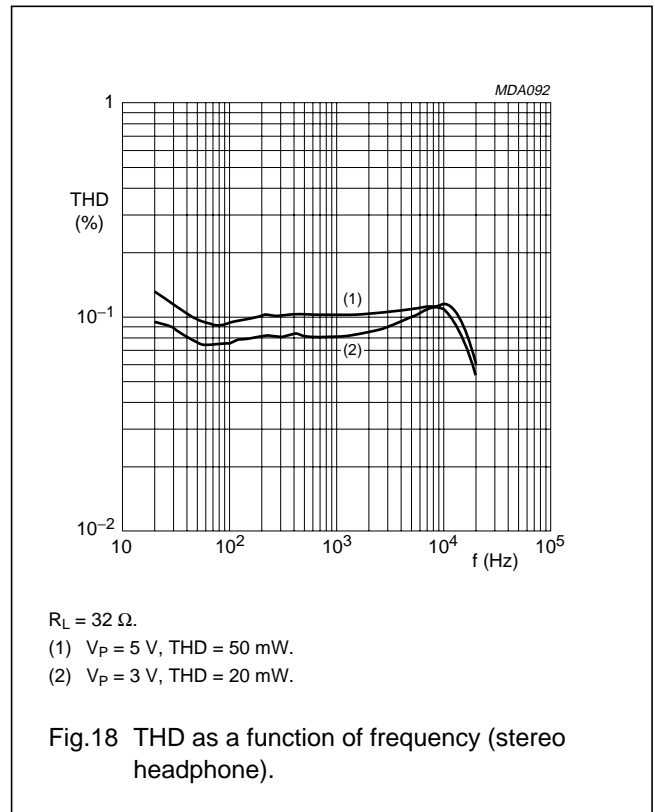
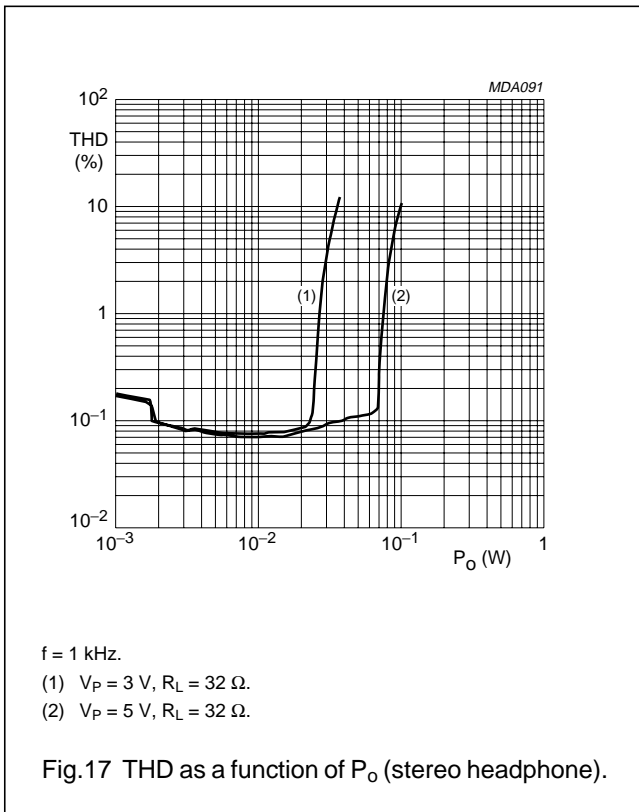
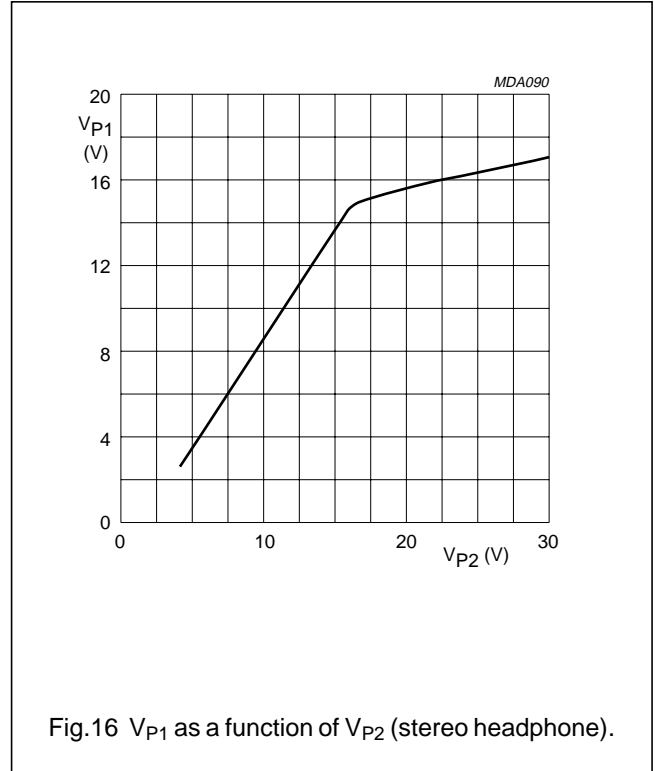
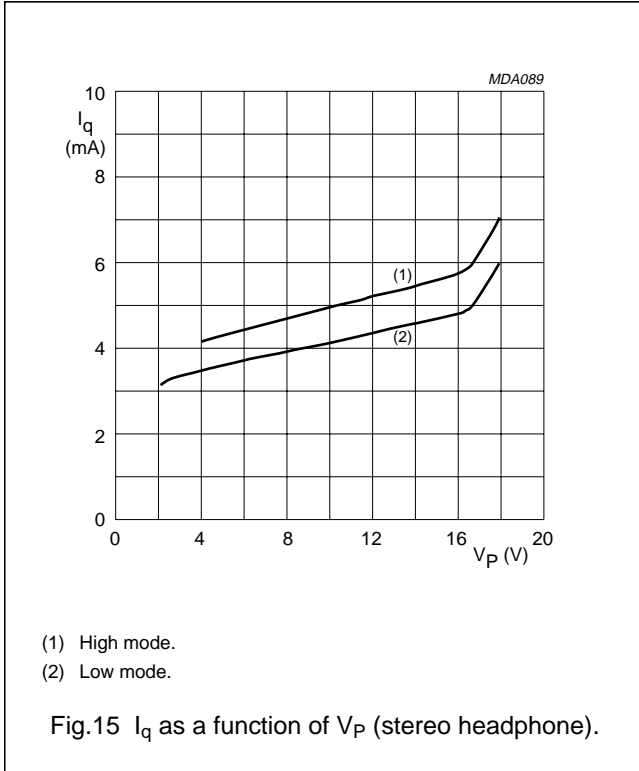


Fig.13 Application 6: Line driver application ($V_P = 6$ to 18 V).

Low-voltage stereo headphone amplifier

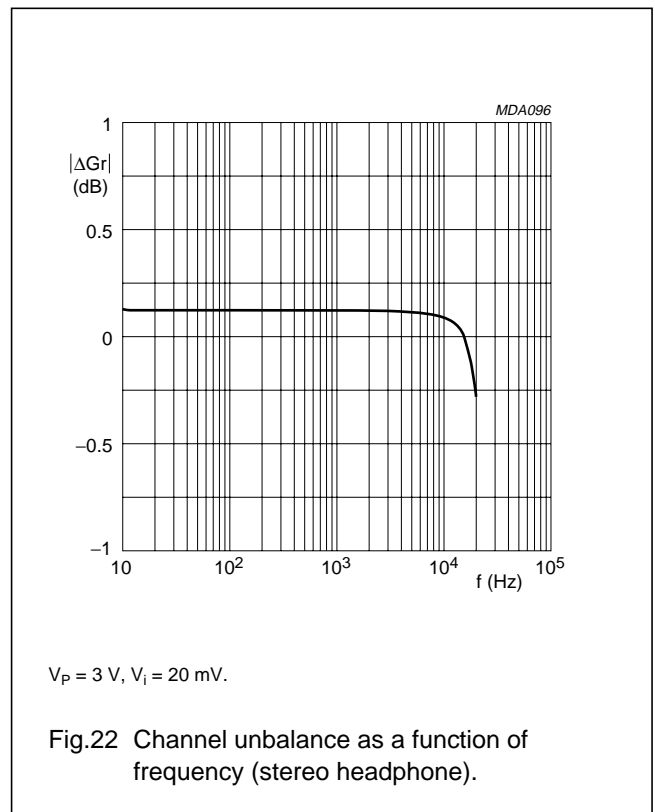
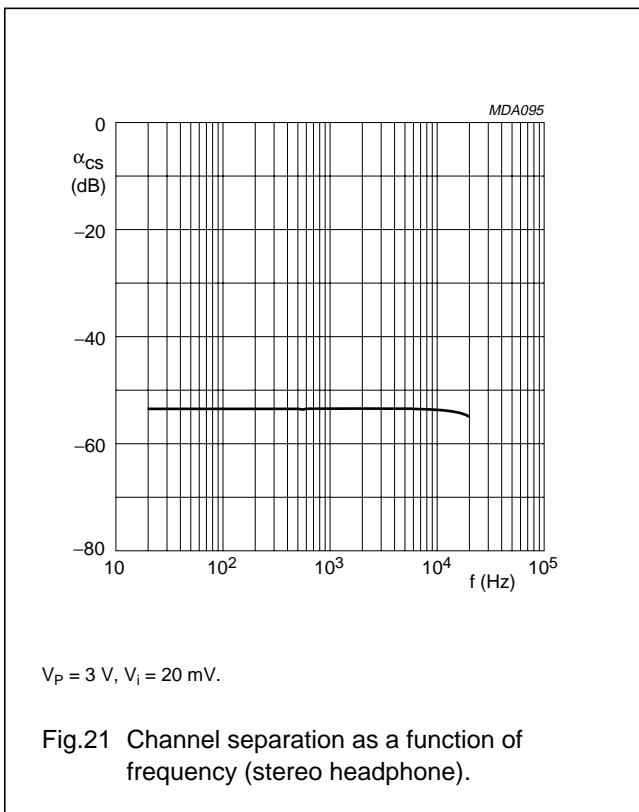
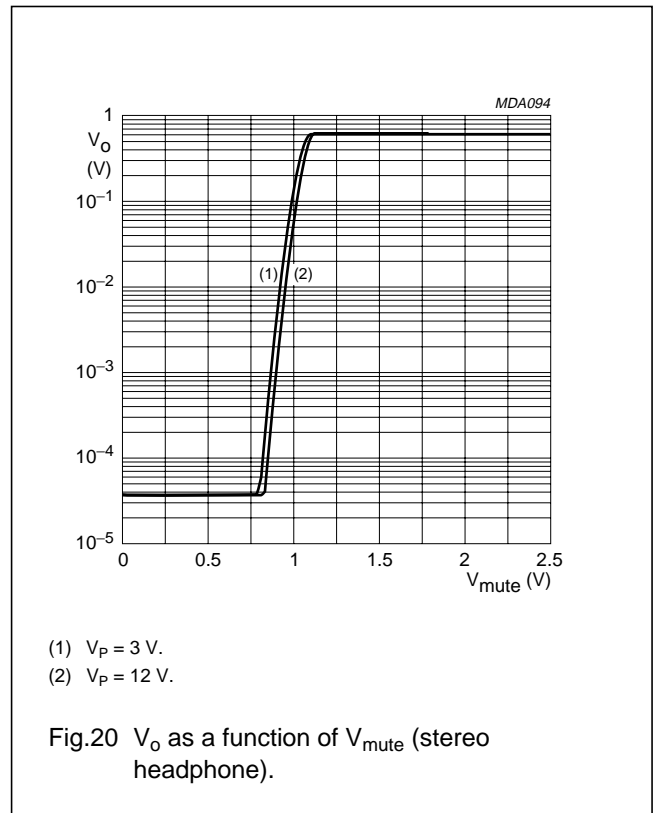
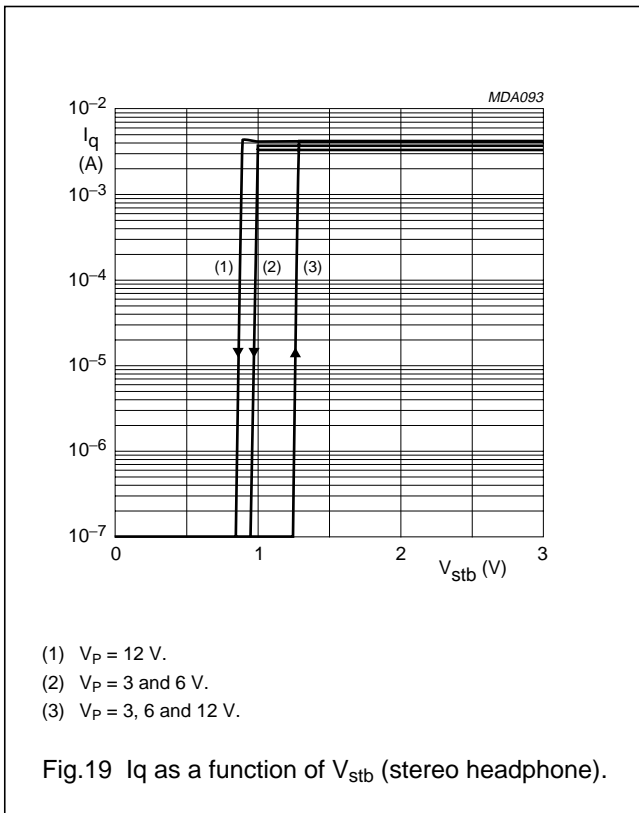
TDA8559

Response curves for low input mode



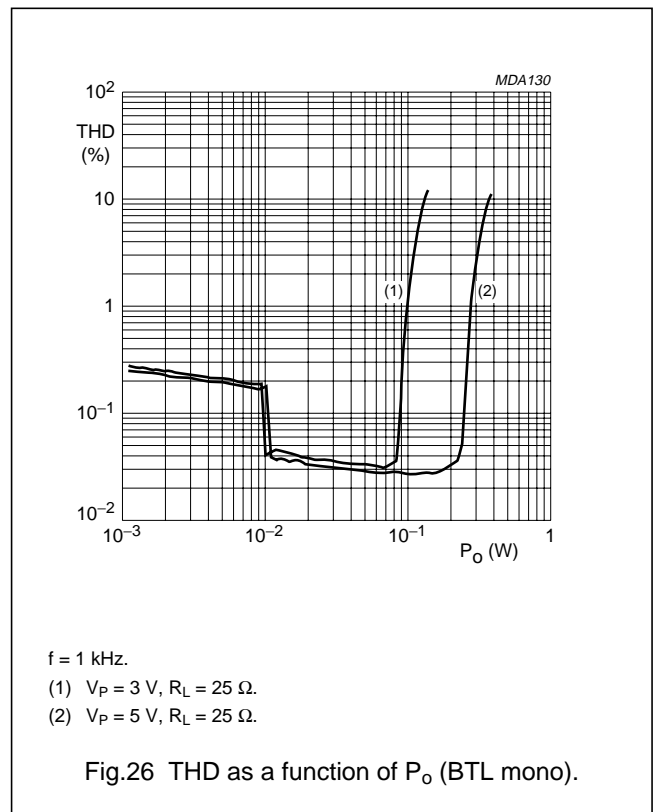
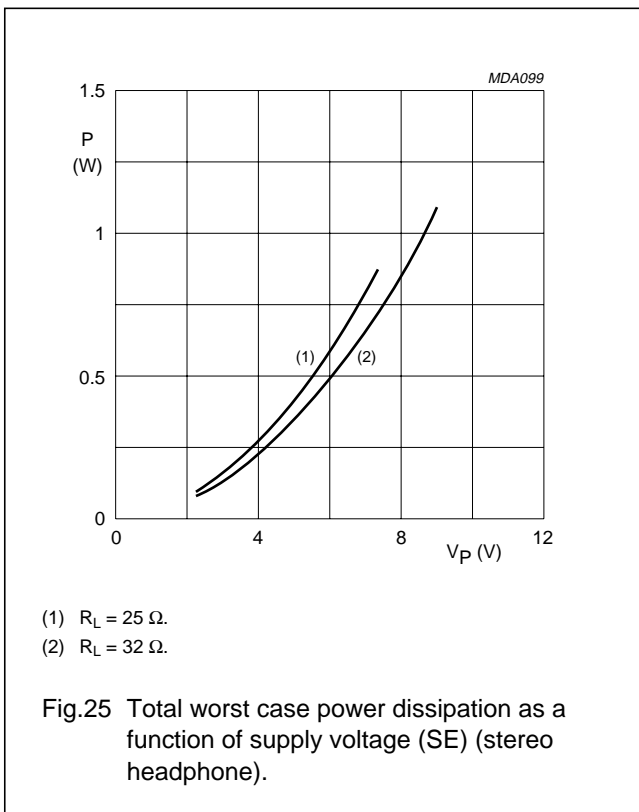
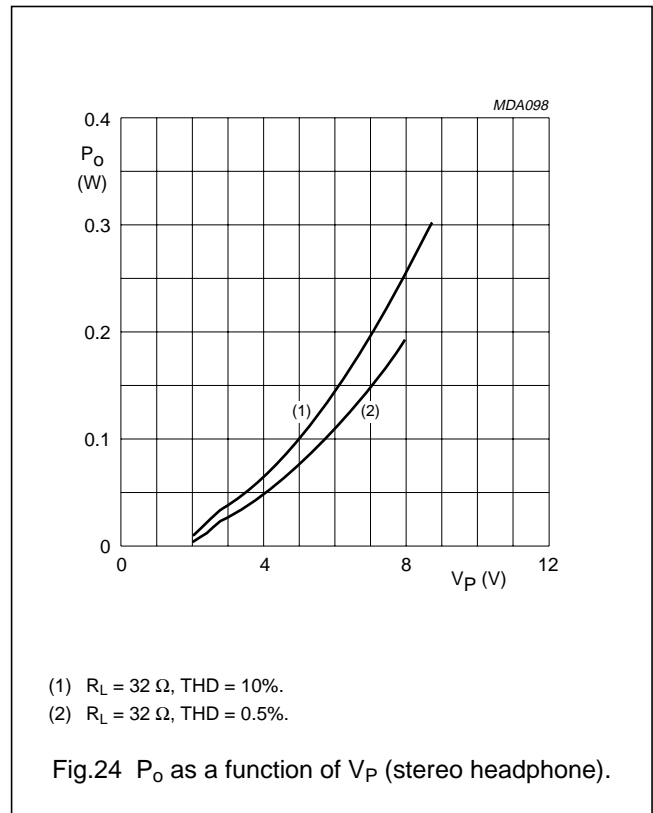
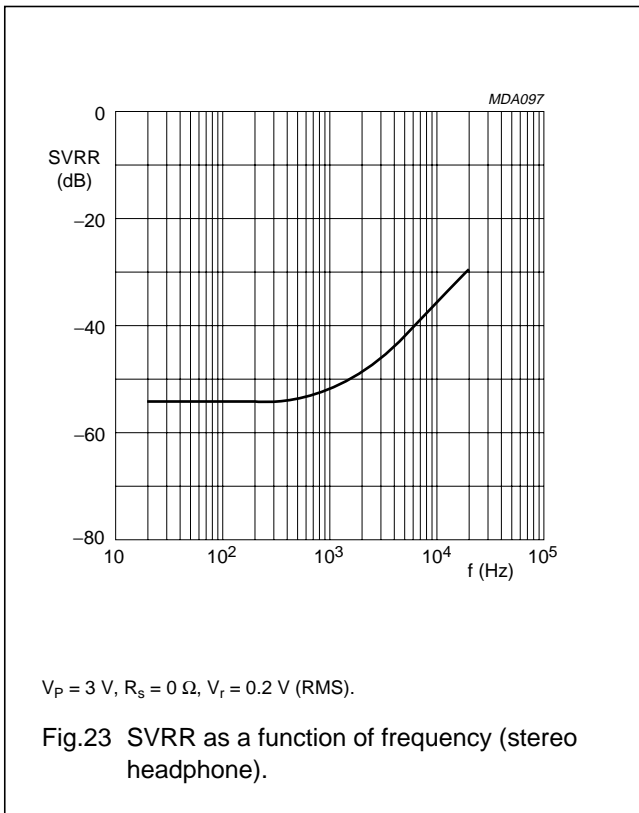
Low-voltage stereo headphone amplifier

TDA8559



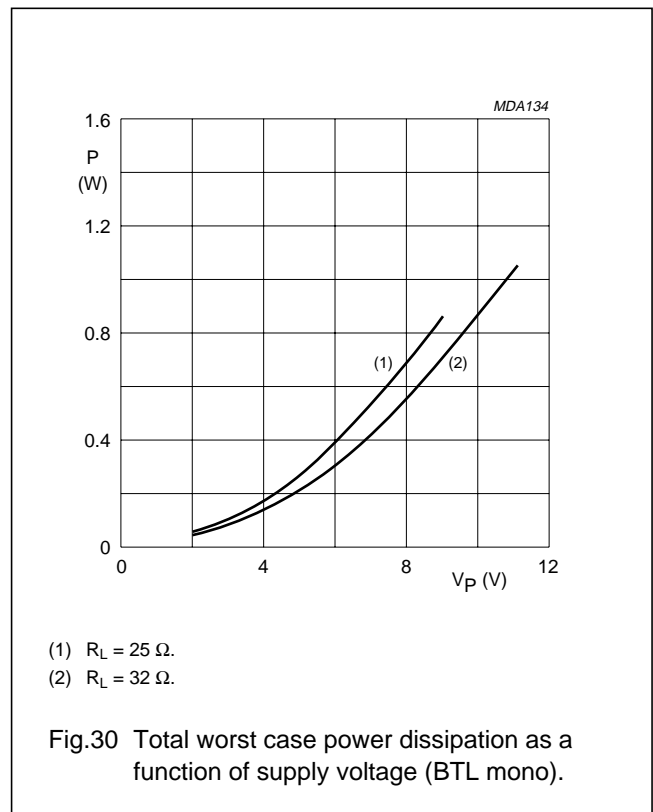
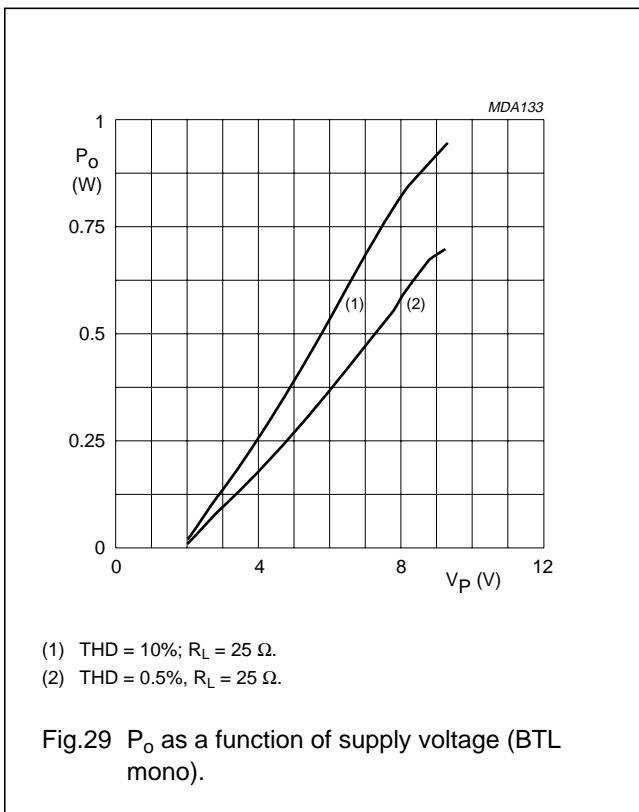
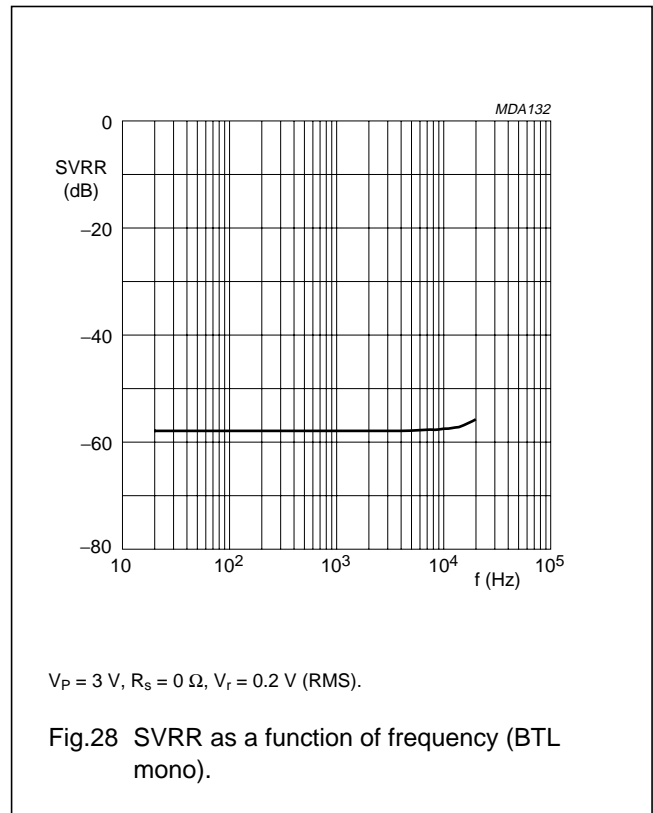
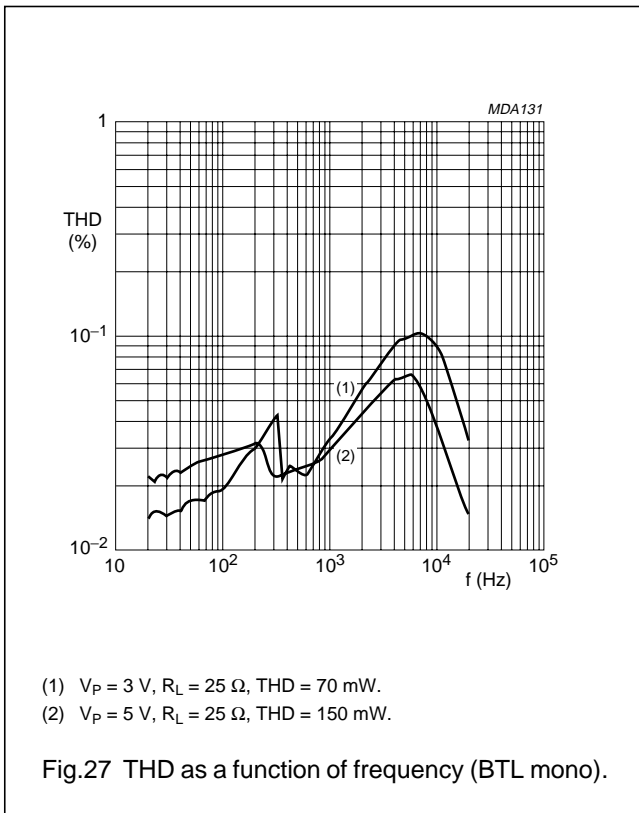
Low-voltage stereo headphone amplifier

TDA8559



Low-voltage stereo headphone amplifier

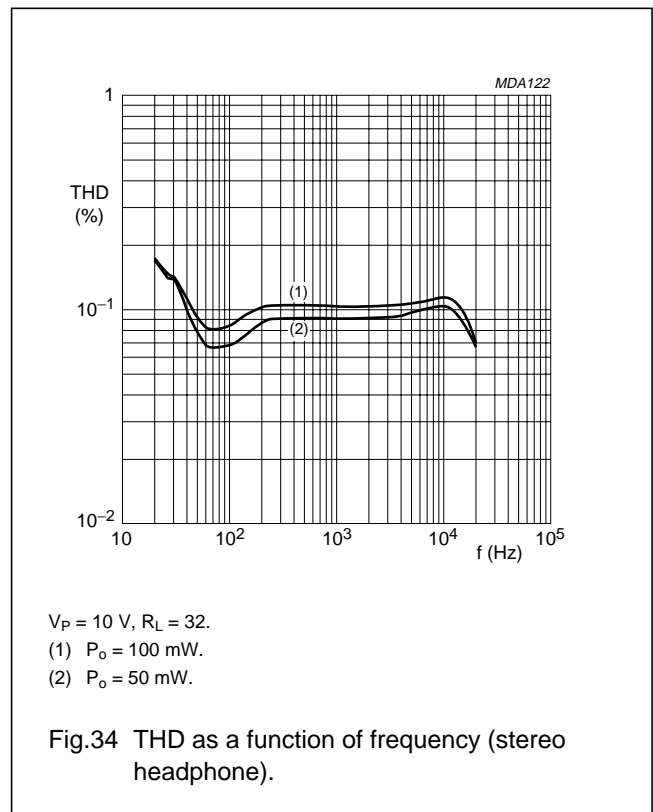
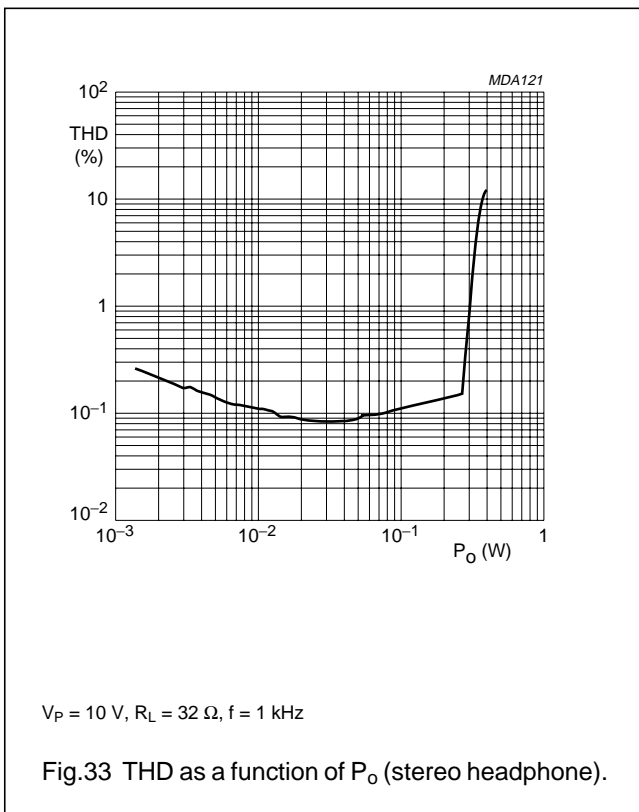
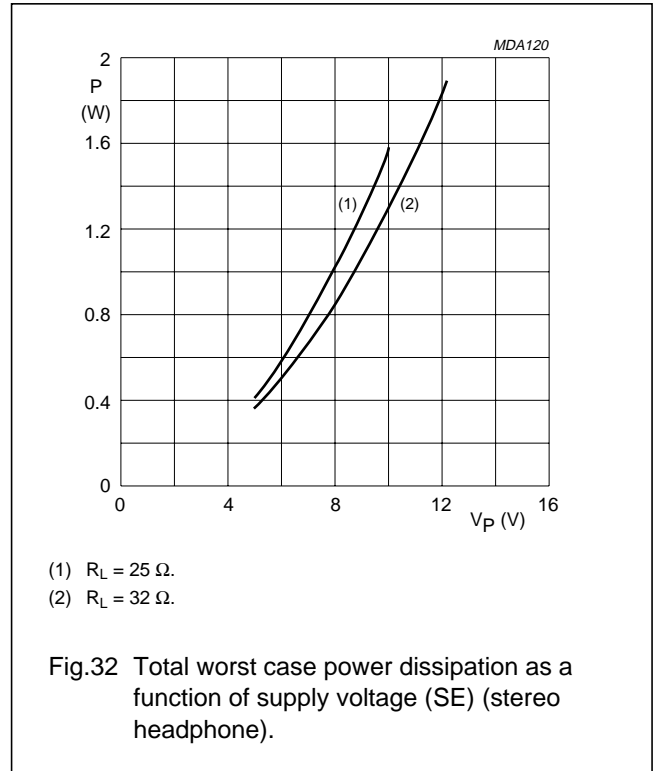
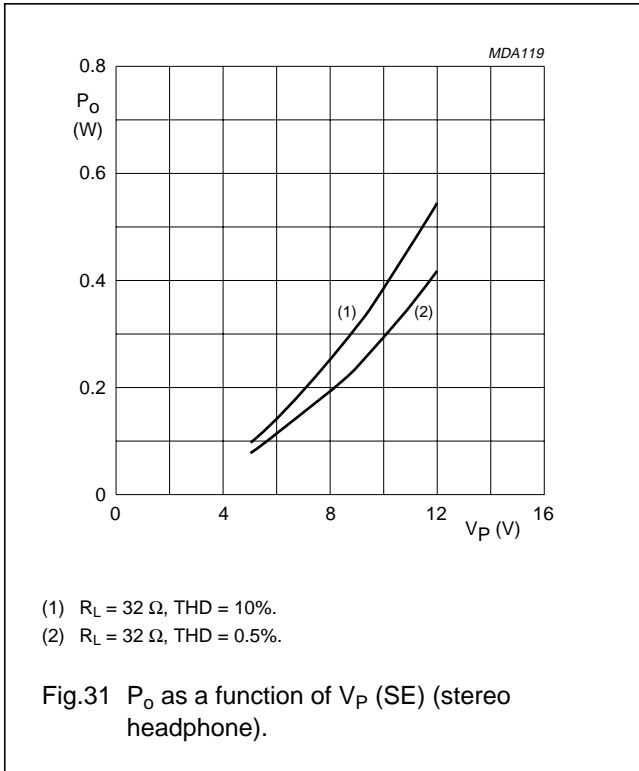
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Low-voltage stereo headphone amplifier

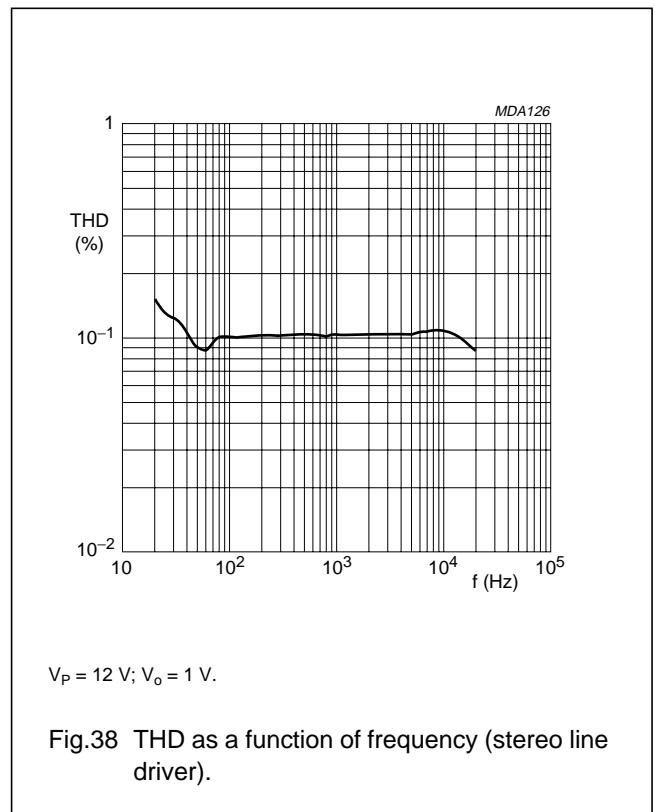
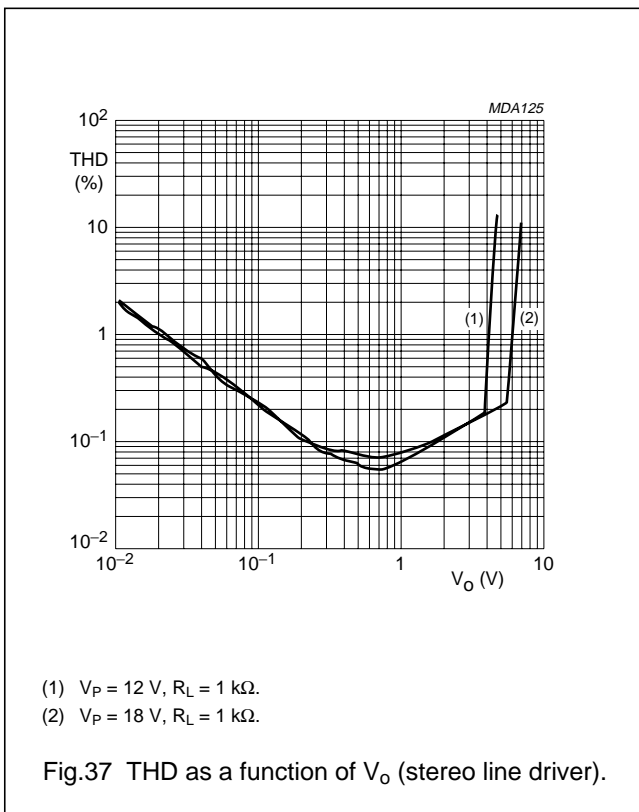
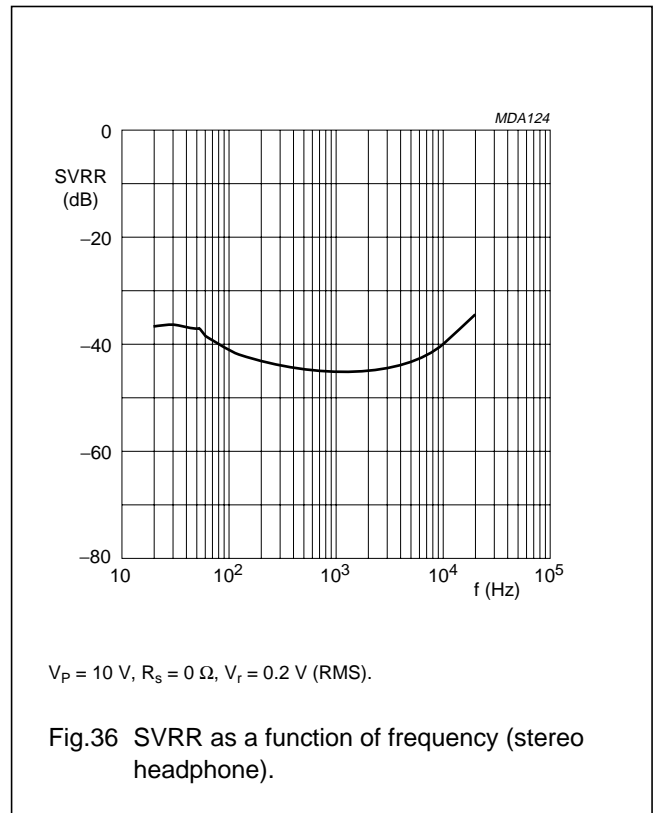
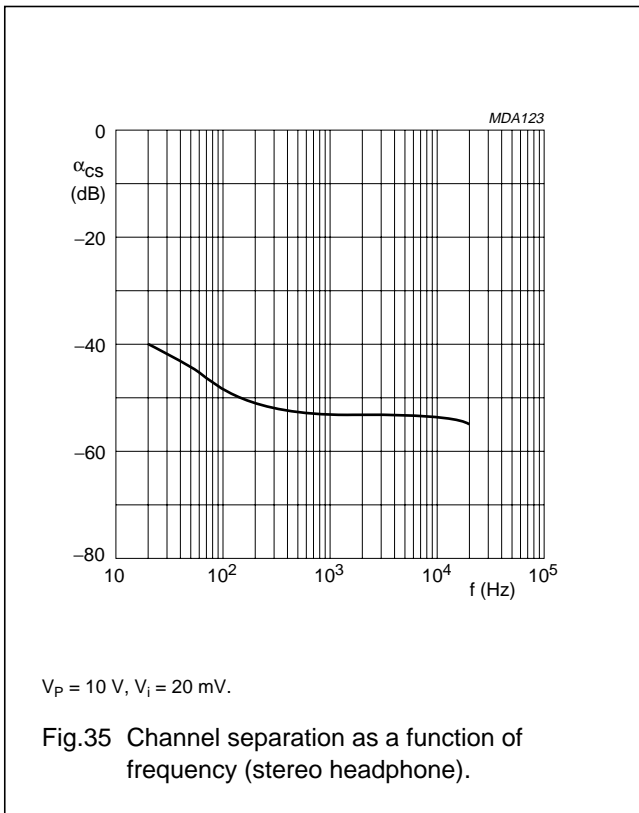
TDA8559

Response curves for high input mode



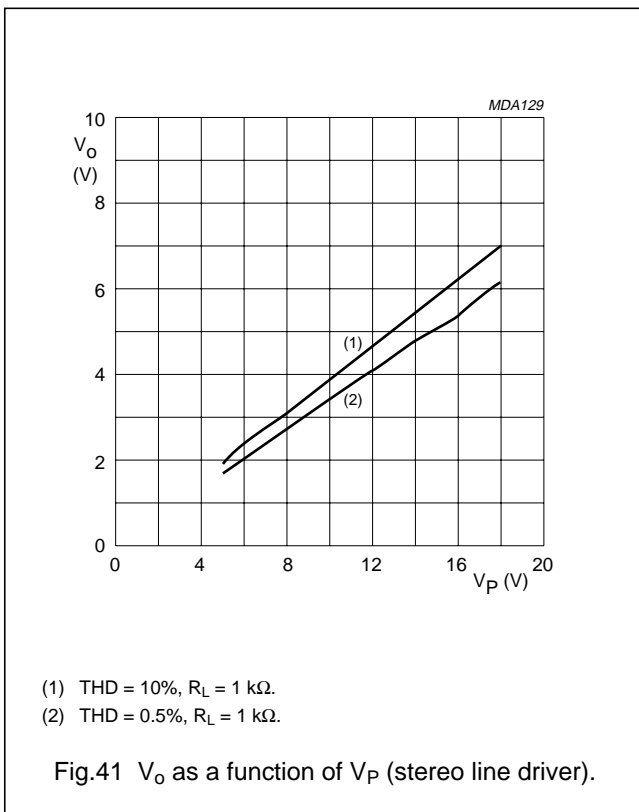
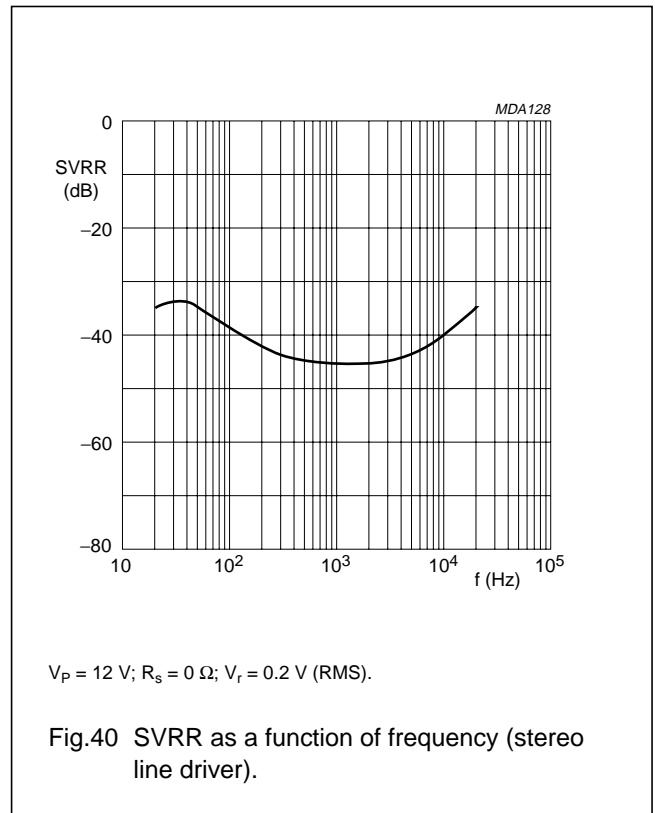
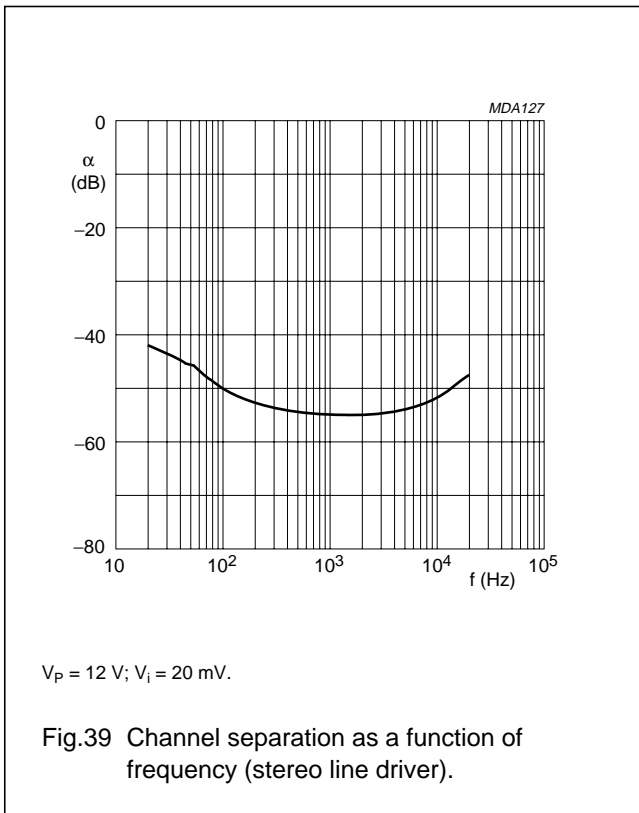
Low-voltage stereo headphone amplifier

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Low-voltage stereo headphone amplifier

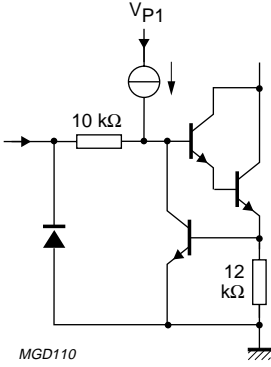
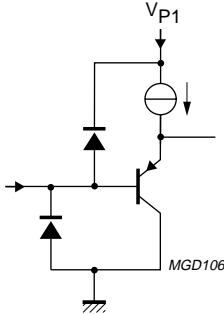
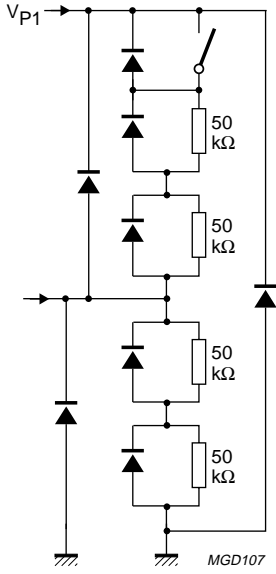
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Low-voltage stereo headphone amplifier

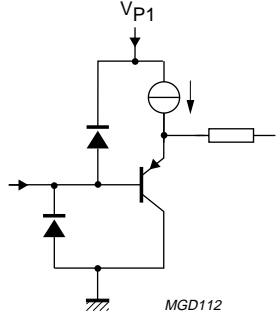
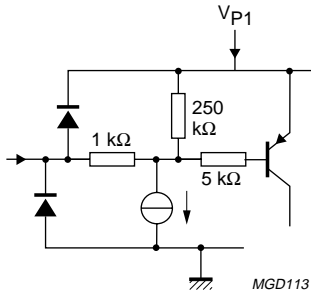
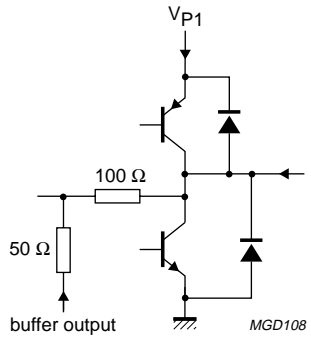
TDA8559

INTERNAL PIN CONFIGURATION

| SYMBOL | PIN | EQUIVALENT CIRCUIT |
|---------------------------|---------------|--|
| STANDBY | 1 |  <p>MGD110</p> |
| +IN1, -IN1, +IN2 and -IN2 | 2, 3, 5 and 6 |  <p>MGD106</p> |
| SVRR | 4 |  <p>MGD107</p> |

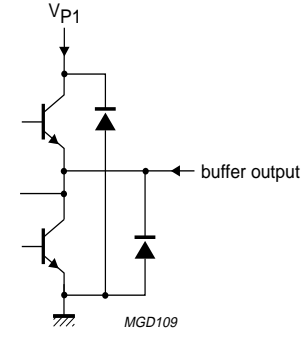
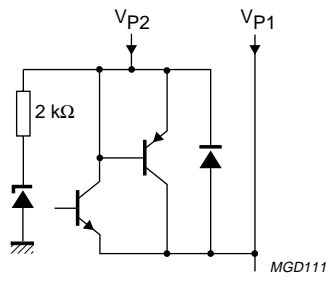
Low-voltage stereo headphone amplifier

TDA8559

| SYMBOL | PIN | EQUIVALENT CIRCUIT |
|---------------|-----------|--|
| MUTE | 7 |  |
| INPUT MODE | 8 |  |
| OUT2 and OUT1 | 11 and 14 |  |

Low-voltage stereo headphone amplifier

TDA8559

| SYMBOL | PIN | EQUIVALENT CIRCUIT |
|-------------|-----------|---|
| BUFFER | 12 |  |
| VP2 and VP1 | 15 and 16 |  |

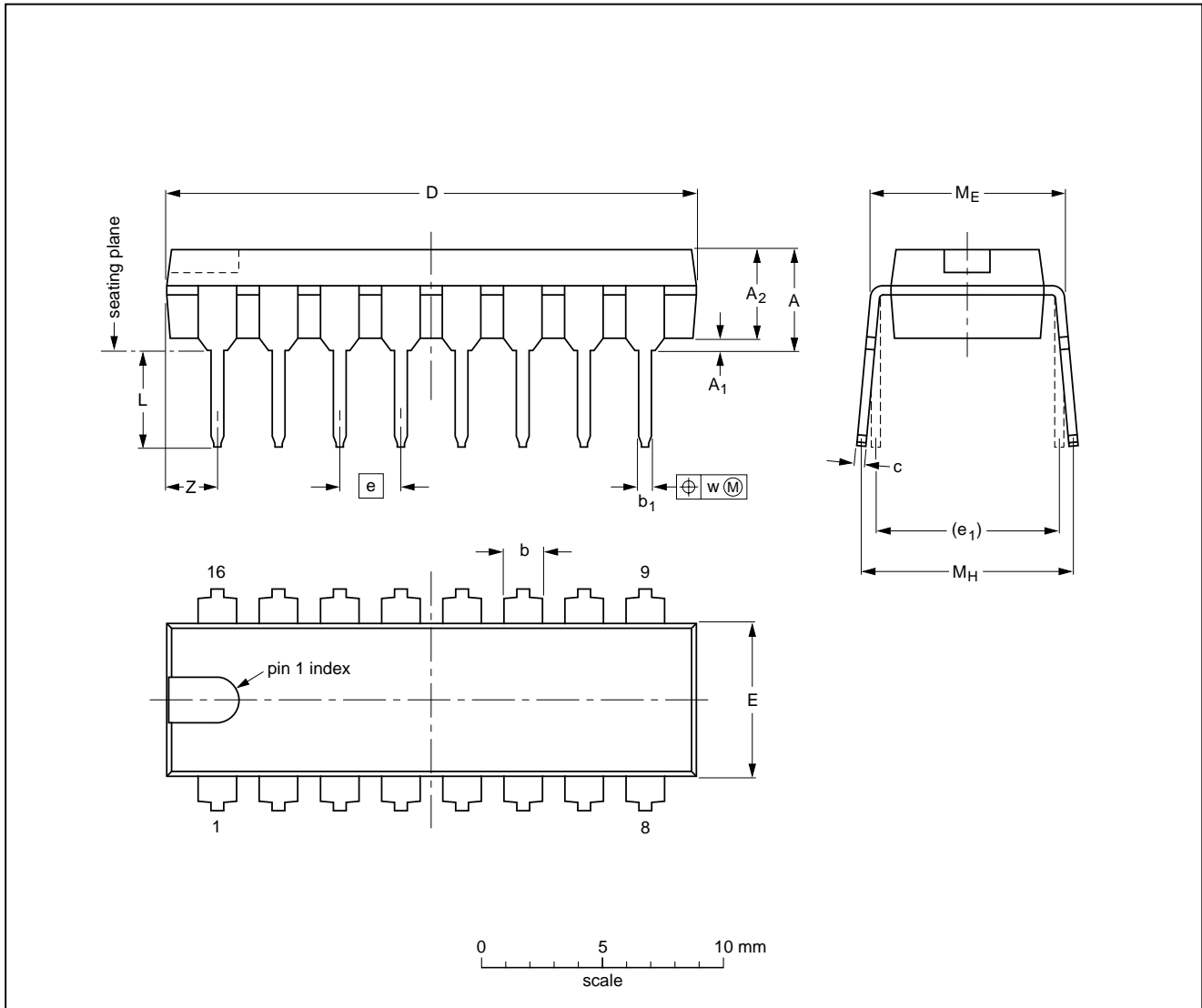
Low-voltage stereo headphone amplifier

TDA8559

PACKAGE OUTLINES

DIP16: plastic dual in-line package; 16 leads (300 mil); long body

SOT38-1



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

| UNIT | A max. | A ₁ min. | A ₂ max. | b | b ₁ | c | D ⁽¹⁾ | E ⁽¹⁾ | e | e ₁ | L | M _E | M _H | w | Z ⁽¹⁾ max. |
|--------|--------|---------------------|---------------------|----------------|----------------|----------------|------------------|------------------|------|----------------|--------------|----------------|----------------|-------|-----------------------|
| mm | 4.7 | 0.51 | 3.7 | 1.40 1.14 | 0.53 0.38 | 0.32 0.23 | 21.8 21.4 | 6.48 6.20 | 2.54 | 7.62 | 3.9 3.4 | 8.25 7.80 | 9.5 8.3 | 0.254 | 2.2 |
| inches | 0.19 | 0.020 | 0.15 | 0.055 0.045 | 0.021 0.015 | 0.013 0.009 | 0.86 0.84 | 0.26 0.24 | 0.10 | 0.30 | 0.15 0.13 | 0.32 0.31 | 0.37 0.33 | 0.01 | 0.087 |

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

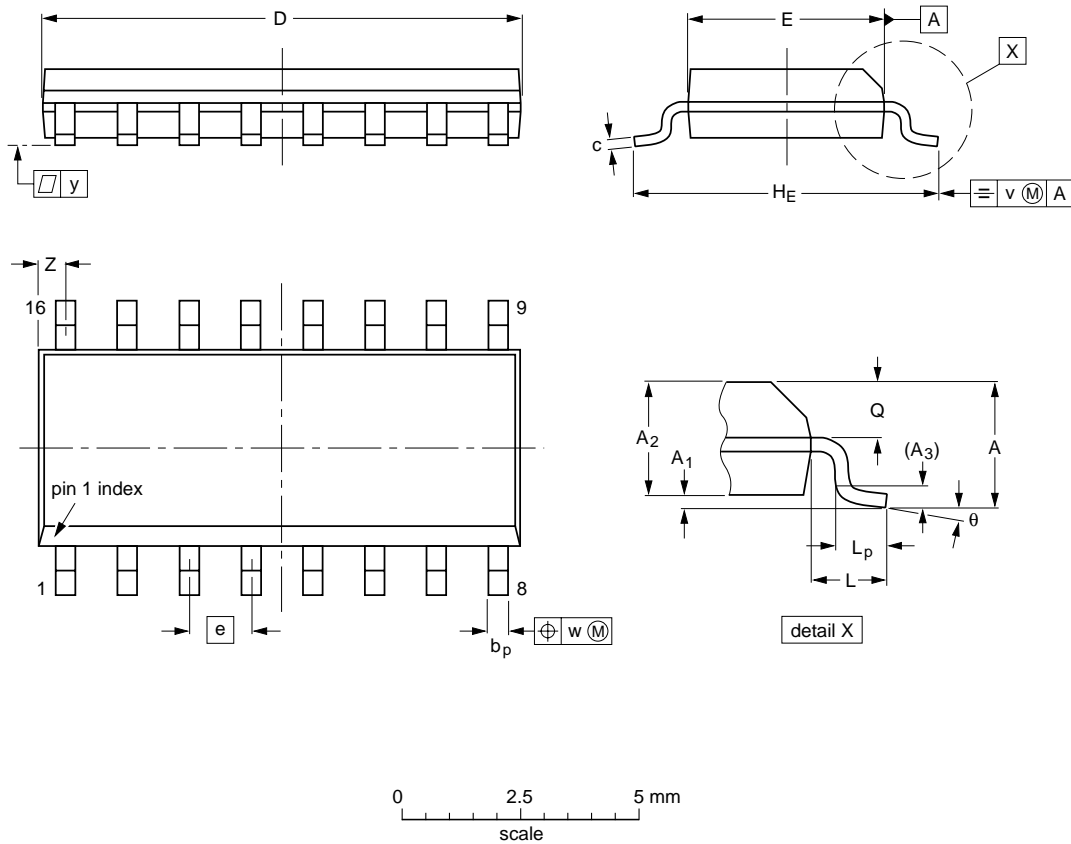
| OUTLINE VERSION | REFERENCES | | | | EUROPEAN PROJECTION | ISSUE DATE |
|-----------------|------------|----------|------|--|---------------------|----------------------|
| | IEC | JEDEC | EIAJ | | | |
| SOT38-1 | 050G09 | MO-001AE | | | | 92-10-02 95-01-19 |

Low-voltage stereo headphone amplifier

TDA8559

SO16: plastic small outline package; 16 leads; body width 3.9 mm

SOT109-1



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

| UNIT | A max. | A ₁ | A ₂ | A ₃ | b _p | c | D ⁽¹⁾ | E ⁽¹⁾ | e | H _E | L | L _p | Q | v | w | y | z ⁽¹⁾ | θ |
|--------|--------|----------------|----------------|----------------|----------------|------------------|------------------|------------------|-------|----------------|-------|----------------|----------------|------|------|-------|------------------|----------|
| mm | 1.75 | 0.25 0.10 | 1.45 1.25 | 0.25 | 0.49 0.36 | 0.25 0.19 | 10.0 9.8 | 4.0 3.8 | 1.27 | 6.2 5.8 | 1.05 | 1.0 0.4 | 0.7 0.6 | 0.25 | 0.25 | 0.1 | 0.7 0.3 | 8° 0° |
| inches | 0.069 | 0.010 0.004 | 0.057 0.049 | 0.01 | 0.019 0.014 | 0.0100 0.0075 | 0.39 0.38 | 0.16 0.15 | 0.050 | 0.244 0.228 | 0.041 | 0.039 0.016 | 0.028 0.020 | 0.01 | 0.01 | 0.004 | 0.028 0.012 | |

Note

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.

| OUTLINE VERSION | REFERENCES | | | | EUROPEAN PROJECTION | ISSUE DATE |
|-----------------|------------|----------|------|--|---------------------|----------------------|
| | IEC | JEDEC | EIAJ | | | |
| SOT109-1 | 076E07S | MS-012AC | | | | 95-01-23 97-05-22 |

Low-voltage stereo headphone amplifier

TDA8559

SOLDERING

Introduction

There is no soldering method that is ideal for all IC packages. Wave soldering is often preferred when through-hole and surface mounted components are mixed on one printed-circuit board. However, wave soldering is not always suitable for surface mounted ICs, or for printed-circuits with high population densities. In these situations reflow soldering is often used.

This text gives a very brief insight to a complex technology. A more in-depth account of soldering ICs can be found in our "IC Package Databook" (order code 9398 652 90011).

DIP

SOLDERING BY DIPPING OR BY WAVE

The maximum permissible temperature of the solder is 260 °C; solder at this temperature must not be in contact with the joint for more than 5 seconds. The total contact time of successive solder waves must not exceed 5 seconds.

The device may be mounted up to the seating plane, but the temperature of the plastic body must not exceed the specified maximum storage temperature ($T_{stg\ max}$). If the printed-circuit board has been pre-heated, forced cooling may be necessary immediately after soldering to keep the temperature within the permissible limit.

REPAIRING SOLDERED JOINTS

Apply a low voltage soldering iron (less than 24 V) to the lead(s) of the package, below the seating plane or not more than 2 mm above it. If the temperature of the soldering iron bit is less than 300 °C it may remain in contact for up to 10 seconds. If the bit temperature is between 300 and 400 °C, contact may be up to 5 seconds.

SO

REFLOW SOLDERING

Reflow soldering techniques are suitable for all SO packages.

Reflow soldering requires solder paste (a suspension of fine solder particles, flux and binding agent) to be applied to the printed-circuit board by screen printing, stencilling or pressure-syringe dispensing before package placement.

Several techniques exist for reflowing; for example, thermal conduction by heated belt. Dwell times vary between 50 and 300 seconds depending on heating method. Typical reflow temperatures range from 215 to 250 °C.

Preheating is necessary to dry the paste and evaporate the binding agent. Preheating duration: 45 minutes at 45 °C.

WAVE SOLDERING

Wave soldering techniques can be used for all SO packages if the following conditions are observed:

- A double-wave (a turbulent wave with high upward pressure followed by a smooth laminar wave) soldering technique should be used.
- The longitudinal axis of the package footprint must be parallel to the solder flow.
- The package footprint must incorporate solder thieves at the downstream end.

During placement and before soldering, the package must be fixed with a droplet of adhesive. The adhesive can be applied by screen printing, pin transfer or syringe dispensing. The package can be soldered after the adhesive is cured.

Maximum permissible solder temperature is 260 °C, and maximum duration of package immersion in solder is 10 seconds, if cooled to less than 150 °C within 6 seconds. Typical dwell time is 4 seconds at 250 °C.

A mildly-activated flux will eliminate the need for removal of corrosive residues in most applications.

REPAIRING SOLDERED JOINTS

Fix the component by first soldering two diagonally-opposite end leads. Use only a low voltage soldering iron (less than 24 V) applied to the flat part of the lead. Contact time must be limited to 10 seconds at up to 300 °C. When using a dedicated tool, all other leads can be soldered in one operation within 2 to 5 seconds between 270 and 320 °C.