Preliminary

Advanced Products

FUJITSU

October 1986
Edition 1.0

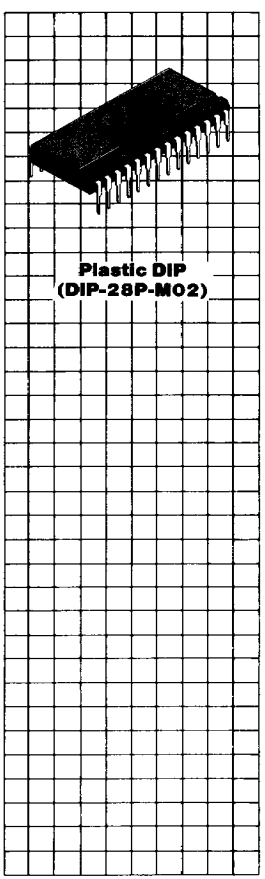
■ MB89311
CMOS Floppy Disk
Controller/Formatter

Description

The Fujitsu MB89311 is a floppy disk controller/formatter (FDC) designed as an enhanced version of the conventional MB8877A.

The MB89311 is designed based on the MB8877A architecture. Some inconveniences of the MB8877A are eliminated on the MB89311, and several new commands are added. It can support micro- (3" or 3.5" double-density), mini- (5.25" double-density), and standard (8" single- or double-density), floppy disk drives. When combined with the MB4107 variable frequency oscillator (VFO), an economical floppy disk drive interface can be created with a minimum of parts.

The MB89311 is fabricated by the silicon-gate CMOS process, and packaged in a 28-pin plastic DIP. It has TTL compatible inputs/outputs. Operation is with a single +5V power supply with low power consumption.



Plastic DIP
(DIP-28P-M02)

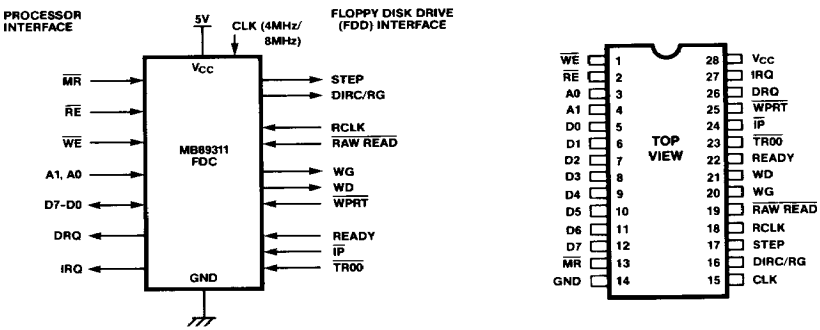
Features

- **Single +5V power supply**
- **TTL compatible I/O**
- **IBM & ISO compatible disk formats**
- **Track seeking with automatic verification**
- **Multiple-sector read/write operation**
- **Track read/write/initialize operation**
- **Program/DMA data transfer**
- **Single density/double density**

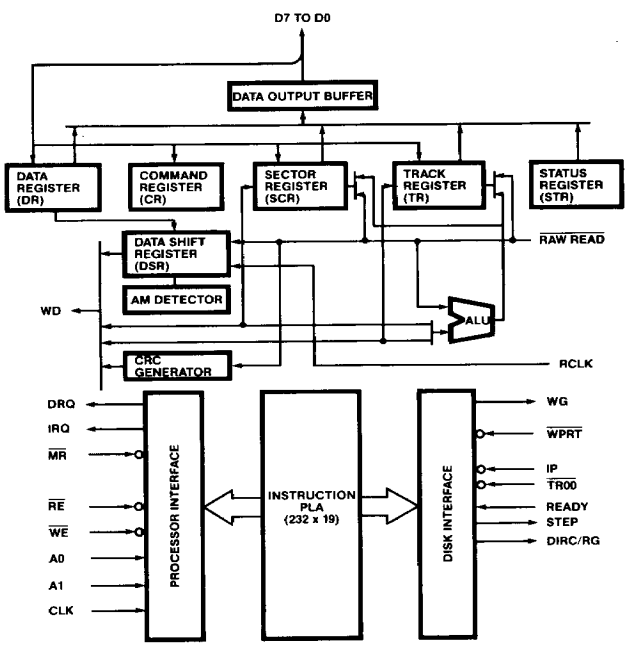
Enhancements

- **Silicon-gate CMOS process**
- **28-pin plastic DIP (Suffix -P)**
- **Built-in programmable write precompensation (125ns/250ns for all tracks at CLK = 8MHz, 250ns/500ns at CLK = 4MHz)**
- **For lost data error, abnormal termination after sector read or write completion**
- **Extended mode commands: Read-after-seek, write-after-seek, delay, and format commands are added.**
- **No restrictions on the RCLK frequency in gap between ID and data fields.**
- **Step rate: 1ms to 30ms, Settling time: 15ms to 60ms**
- **Record length: 128, 256, 512, 1024, 2048, 4096, and 8192 bytes/sector**

Logic Symbol and Pin Assignment



Block Diagram



This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

Pin Descriptions

The MB89311 FDC has two interfaces: One is the processor interface; MR, RE, WE, and A1 & A0 inputs, D7–D0 inputs/outputs, and DRQ & IRQ outputs which are used for the processor to control the FDC. The other is the floppy disk drive (FDD) interface; STEP, DIREC/RG, WG, and WD outputs, and RCLK, RAW READ, WPRT, READY, TR00, IP inputs, which are used for the FDC to control the FDD.

	Symbol	Number	Type	Name & Function
Power Supply & Clock	V_{CC}	28	—	+5Vdc power supply pin.
	V_{SS}	14	—	Power supply ground pin.
	CLK	15	I	Clock input: Basic timing clock for internal circuits. 8MHz and 4MHz frequencies are required for 500K bits/s data transfer rate in MFM (250K bits/s in FM) and 250K bits/s in MFM (125K bits/s in FM). The CLK signal is required also during a reset.
Processor Interface	$\overline{MR}$	13	I	Master Reset: A low level on this pin stops FDC operation, and initializes its internal state. The CLK signal is required also during a reset.
	$\overline{RE}$	2	I	Read Enable: Strobe signal for reading data from the internal register addressed by A1 and A0.
	$\overline{WE}$	1	I	Write Enable: Strobe signal for writing data into the internal register addressed by A1 and A0.
	A1, A0	4, 3	I	Register Select Line: Signal for addressing an internal register (CR, STR, TR, SCR, or DR).
	D7–D0	12–5	I/O	Data Access Line: 8-bit bidirectional three-state data bus. These lines go to a high impedance state when $\overline{RE}$ and $\overline{WE}$ are high.
	DRQ	26	O	Data Request: Notifies the processor when new data must be read from or written into the data register. This pin is an open-drain output and must be pulled up by an external 10kΩ resistor.
	IRQ	27	O	Interupt Request: Set when a command completes, terminates, or a force interrupt command is specified. This pin is an open-drain output and must be pulled up by an external 10kΩ resistor. Undefined at power-on.
Floppy Disk Drive Interface	STEP	17	O	Step: Signal for moving disk head. One pulse is generated to move the head by one track.
	DIRC/RG	16	O	Direction/Read Gate: During disk head operations, when this signal is low, the head moves to the outside, and when high, to the inside. During read operations, when this signal is high, it indicates that read data has been synchronized.
	RCLK	18	I	Read Clock: A data window signal for the raw read data from disk. This signal is generated by an external VFO circuit.
	$\overline{RAW\ READ}$	19	I	Raw Read Data: Serial raw data read from disk, containing clock and data bits.
	WG	20	O	Write Gate: This signal is high when valid data is being written to disk.
	WD	21	O	Write Data: Serial write data pulses to be written to disk.
	$\overline{WPRT}$	25	I	Write Protect: Signal for inhibiting write operation to disk. When this signal is low, write operation is disabled.
	READY	22	I	Ready: When this signal is high, the disk drive is ready for operation. Commands except for Type I commands can be executed if this signal is high.
	$\overline{TR00}$	23	I	Track 00: When this signal is low, it indicates that the disk head is positioned at track 00.
	$\overline{IP}$	24	I	Index Pulse: Pulsed low each time the index hole of the floppy disk is detected.

Functional Description

Register Set

The MB89311 FDC contains the following five registers to execute commands and indicate status:

- Command register (CR)
- Status register (STR)
- Track register (TR)
- Sector register (SR)
- Data register (DR)

These registers are addressed by register select lines A1 and A0 under RE and WE control.

Register Selection

A1	A0	Read Mode ($\overline{RE}$ = 0)	Write Mode ($\overline{WE}$ = 0)
0	0	Status register	Command register
0	1	Track register	Track register
1	0	Sector register	Sector register
1	1	Data register	Data register

Command Words

The FDC's operations are defined by commands, that are divided into four groups: Types I, II, III, and IV. Each group contains one to five command(s). Each command has flags that define detailed operation of the command.

The FDC has two command modes, the 8877 mode (which emulates the MB8877 command set) and the extended mode (in which additional commands can be used). Either of these two modes can be selected by the assign command.

Command Summary (1): 8877 Mode Command Set

Type	Name	Code MSB							LSB	Function
I	Restore	0	0	0	0	X	V	r1	r0	Moves head to track 0.
	Seek	0	0	0	1	X	V	r1	r0	Moves head to a desired track.
	Step	0	0	1	u	X	V	r1	r0	Moves head one track.
	Step-in	0	1	0	u	X	V	r1	r0	Moves head one track to inside.
	Step-out	0	1	1	u	X	V	r1	r0	Moves head one track to outside.
II	Read data	1	0	0	m	S	E	C	L	Reads data (data field) from disk.
	Write data	1	0	1	m	S	E	C	a0	Writes data (data field) to disk.
III	Read address	1	1	0	0	0	E	0	0	Reads ID field from disk.
	Read track	1	1	1	0	0	E	0	0	Reads all data from one track.
	Write track	1	1	1	1	0	E	0	0	Writes all data to one track.
IV	Assign parameter	1	1	1	1	1	1	0	1	Selects operation timing.
	Assign mode	1	1	1	1	1	1	1	0	Selects operation mode.
	Force interrupt	1	1	0	1	I3	I2	I1	I0	Generates interrupt (IRQ).

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Functional Description
(Continued)

Command Summary (2): Extended Mode Command Set

Type	Name	Code MSB							LSB	Function
I	Restore	0	0	0	0	0	V	0	0	Moves head to track 0.
	Seek	0	0	0	1	0	V	0	0	Moves head to a desired track.
	Step	0	0	1	u	0	V	0	0	Moves head one track.
	Step-in	0	0	1	u	0	V	0	1	Moves head one track to inside.
	Step-out	0	0	1	u	0	V	1	0	Moves head one track to outside.
II	Read-after-seek	0	1	0	0	S	1	C	L	Reads one sector data after seek.
	Write-after-seek	0	1	1	0	S	1	C	a0	Writes one sector data after seek.
	Read data	1	0	0	m	S	E	C	L	Reads data (data field) from disk.
	Write data	1	0	1	m	S	E	C	a0	Writes data (data field) to disk.
III	Read address	1	1	0	0	0	E	0	0	Reads ID field from disk.
	Read track	1	1	1	0	0	E	0	0	Reads all data from one track.
	Write track	1	1	1	1	0	E	0	0	Writes all data to one track.
	Format	1	1	1	1	0	E	0	1	Formats disk.
IV	Delay	1	1	1	1	1	1	0	0	Generates interrupt after a set time.
	Assign parameter	1	1	1	1	1	1	0	1	Selects operation timing.
	Assign mode	1	1	1	1	1	1	1	0	Selects operation mode.
	Reset	1	1	1	1	1	1	1	1	Resets FDC.
	Force interrupt	1	1	0	1	I3	I2	I1	I0	Generates interrupt (IRQ).

Flag Summary

Type	Symbol	Function
I	u	Update of track register
	V	Verify at destination track
	r1, r0	Step rate of STEP pulse
II	m	Multiple sectors
	S	Side number
	a0	Data address mark
III	C	Side compare
	L	Long read (CRC read)
IV	I3-I0	Interrupt

Functional Description

Status Words

Status words, which are automatically held in the status register, show the status of the executing command, executed command, and conditions of the FDD. The system processor can monitor the FDC operations and FDD conditions, reading the status register.

When the FDC receives a command, the status register is automatically preset at the start of the command execution. Each status bit is internally updated (set or reset) during the command execution, and the status word is established at the completion of the command.

Status Word Summary

Command		Status Bit STR7	STR6	STR5	STR4	STR3	STR2	STR1	STR0
Type I	All commands	Not Ready	Write Protect	1	Seek Error	CRC Error	Track 00	Index	Busy
Type II	Read data & Read-after-seek	Not Ready	D/M N/F	Rec. Type	Rec. N/F	CRC Error	Lost Data	Data Request	Busy
	Write data & Write-after-seek	Not Ready	0	0	Rec. N/F	CRC Error	Lost Data	Data Request	Busy
Type III	Read address	Not Ready	0	0	Rec. N/F	CRC Error	Lost Data	Data Request	Busy
	Read track	Not Ready	Write Protect	0	0	0	Lost Data	Data Request	Busy
	Write track	Not Ready	Write Protect	0	0	0	Lost Data	Data Request	Busy
	Format	Not Ready	Write Protect	0	0	Illegal Length	Lost Data	Data Request	Busy
Type IV	Force Interrupt	In accordance with the executing commands.							0
		Not Ready	Write Protect	0	0	0	Track 00	Index	0
	Reset command & Master reset	In accordance with Type I commands.							
	Delay, Assign Parameter & Mode	Not Ready	0	0	0	0	0	0	Busy

Notes: Rec. = Record, N/F = Not Found
D/M N/F = Data Mark Not Found. This status bit is valid in extended mode only. In 8877 mode, this bit is "0".

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Functional Description (Continued)

Status Bit Function Summary

Command	Status	Status Bit	Function
Type I	Not Ready	STR7	1 = FDD is not ready: Not Ready = $\overline{\text{READY}}$ + MR.
	Write Protect	STR6	1 = Write operation is inhibited: Write Protect = WPRT.
	Seek Error	STR4	1 = Verify operation was unsuccessful.
	CRC Error	STR3	1 = CRC check error occurred.
	Track 00	STR2	1 = Disk head is positioned at track 0: Track 00 = TR00.
	Index	STR1	1 = Index hole was detected. Index = INP
	Busy	STR0	1 = FDC is executing a command.
Type II & Type III	Not Ready	STR7	1 = FDD is not ready. Not Ready = $\overline{\text{READY}}$ + MR.
	Write Protect	STR6	1 = Write operation is inhibited. Write Protect = WPRT.
	Data Mark Not Found*		1 = Data mark was not found within required byte interval after ID mark detection.
	Record Type	STR5	1 = Data address mark was deleted data mark.
	Record Not Found	STR4	1 = Desired track and sector were not found.
	CRC Error	STR3	1 = CRC check error occurred.
	Lost Data	STR2	1 = Data was not read from or written to data register within required time interval.
	Data Request	STR1	1 = DRQ is currently active. Data Request = DRQ.
	Busy	STR0	1 = FDC is executing a command.

*For read data and read-after-seek commands in extended mode only.

Absolute Maximum Ratings (Note)

Parameter	Symbol	Rating Min	Rating Max	Unit	Note
Supply Voltage	V_{CC}	V_{SS}–0.3	V_{SS}+7.0	V	
	V_{SS}		0	V	
Input Voltage	V_{IN}	V_{SS}–0.3	V_{SS}+7.0	V	Should not exceed V_{CC}+0.5V
Output Voltage	V_{OUT}	V_{SS}–0.3	V_{SS}+7.0	V	Should not exceed V_{CC}+0.5V
Operating Temperature	T_A	–40	+85	°C	
Storage Temperature	T_{STG}	–55	+150	°C	

Note: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Recommended Operating Conditions

Parameter	Symbol	Value Min	Value Typ	Value Max	Unit	Note
Supply Voltage	V_{CC}	4.5	5.0	5.5	V	
	V_{SS}		0		V	
Operating Temperature	T_A	–40		+85	°C	

DC Characteristics

(Recommended operating conditions unless otherwise noted).
(V_{CC} = +5V ± 10%, GND = 0V, T_A = -40°C to +85°C)

Parameter	Symbol	Value Min	Value Max	Unit	Test Condition
Input Low Voltage	V_{IL}	-0.3	0.8	V	
Input High Voltage	V_{IH}	2.2	V_{CC}	V	
Output Low Voltage	V_{OL}		0.45	V	I_{OL} = 2.5mA
Output High Voltage	V_{OH}	2.4		V	I_{OH} = -400μA
		V_{CC}-0.4		V	I_{OH} = -100μA
Input Leakage Current	I_{IL}	-10	+10	μA	$0V \leq V_{IN} \leq V_{CC}$
Output Leakage Current	I_{OFL}	-10	+10	μA	$0V \leq V_{OUT} \leq V_{CC}$
Standby Current	I_{CC}		10	mA	
Input Capacitance	C_{IN}		10	pF	V_{CC} = GND = 0V, T_A = 25°C, All pins except measured pin are 0V
Output Capacitance	C_{OUT}		20	pF	
I/O Capacitance	$C_{I/O}$		20	pF	

AC Characteristics

(Recommended operating conditions unless otherwise noted).
(V_{CC} = +5V ± 10%, GND = 0V, T_A = -40°C to +85°C)

CPU Read Timing (from FDC)

Parameter	Symbol	Value Min	Value Max	Unit	Test Condition
Address Setup Time (to $\overline{RE}$↓)	t_{SET}	50		ns	
Address Hold Time (from $\overline{RE}$↓)	t_{HLD}	15		ns	
$\overline{RE}$ Pulse Width	t_{RE}	150		ns	
Data Delay Time (from $\overline{RE}$↓)	t_{DACC}		120	ns	C_L = 150pF
Data Hold Time (from $\overline{RE}$↑)	t_{DOH}	10	75	ns	C_L = 150pF
DRQ Service Time (from DRQ to $\overline{RE}$↑)	t_{SEVR}		13.5	μs	t_C = 2μs
DRQ Release Time (from $\overline{RE}$↓ to DQR↓)	t_{DRR}		150	ns	
IRQ Release Time (from $\overline{RE}$↓ to IRQ↓)	t_{IRR}		500	ns	

CPU Write Timing (to FDC)

Parameter	Symbol	Value Min	Value Max	Unit	Test Condition
Address Setup Time (to $\overline{WE}$↓)	t_{SET}	50		ns	
Address Hold Time (from $\overline{WE}$↑)	t_{HLD}	10		ns	
$\overline{WE}$ Pulse Width	t_{WE}	100		ns	
Data Setup Time (to $\overline{WE}$↑)	t_{DS}	100		ns	
Data Hold Time (from $\overline{WE}$↑)	t_{DH}	0		ns	
DRQ Service Time (from DRQ to $\overline{WE}$↑)	t_{SEVW}		9.5*	μs	
DRQ Release Time (from $\overline{WE}$↓ to DQR↓)	t_{DRR}		150	ns	
IRQ Release Time (from $\overline{WE}$↓ to IRQ↓)	t_{IRR}		500	ns	

* This value is doubled when CLK = 4MHz.

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AC Characteristics
(Continued)
(Recommended operating conditions unless otherwise noted.)
(V_{CC} = +5V ± 10%, GND = 0V, T_A = −40° C to +85° C)

FDC Read Timing (from FDD)

Parameter	Symbol	Value Min	Value Typ	Value Max	Unit	Test Condition
RAW READ Pulse Width	t_{PW}	100			ns	
RAW READ Cycle Time	t_{BC}		*2,*3,*4		μs	MFM
			*2, *4			FM
RCLK Setup Time (from RCLK Change to to RAW READ↓)	t_D	40			ns	
RCLK Hold Time (from RAW READ↓ to RCLK Change)	t_{CD}	40			ns	
RCLK High Time	t_A	0.8	1*	8	μs	MFM
		0.8	2*	8		FM
RCLK Low Time	t_B	0.8	1*	8	μs	MFM
		0.8	2*	8		FM
RCLK Cycle Time	t_C		2*		μs	MFM
			4*			FM

* These values are doubled when the CLK = 4MHz.

FDC Write Timing (to FDD)

Parameter	Symbol	Value Min	Value Typ	Value Max	Unit	Test Condition
WD Pulse Width	t_{WD}	450	500	550	ns	CLK=8MHz, FM
		200	250	300		CLK=8MHz, MFM
WG Setup Time (from WG↑ to WD↑)	t_{WG}		2		μs	CLK=8MHz, FM
			1			CLK=8MHz, MFM
WG Hold Time (from WD↓ to WG↓)	t_{WF}		2		μs	CLK=8MHz, FM
		1		2		CLK=8MHz, MFM
WD Output Delay	t_{CWD}	20		100	ns	

AC Characteristics

(Continued)
(Recommended operating conditions unless otherwise noted.)
(V_{CC} = +5V ± 10%, GND = 0V, T_A = −40°C to +85°C)

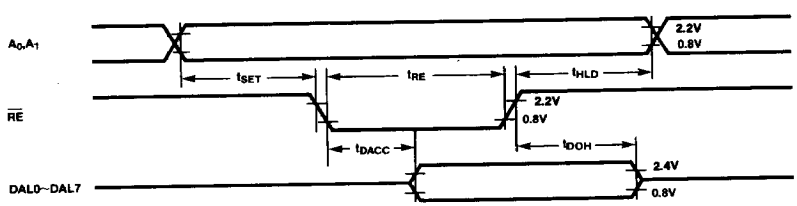
Other Timing

Parameter	Symbol	Value Min	Value Typ	Value Max	Unit	Test Condition
CLK Cycle Time	t_{CYC}	125		500	ns	
CLK Low Time	t_{CD1}	55		250	ns	
CLK High Time	t_{CD2}	55		250	ns	
STEP Pulse Width	t_{STP}	6*			μs	MFM
		12*				FM
DIRC Setup Time	t_{DIRS}	12*			μs	
DIRC Hold Time	t_{DIRH}	6*			μs	
$\overline{MR}$ Pulse Width	t_{MR}	50*			μs	
$\overline{IP}$ Pulse Width	t_{IP}	10*			μs	

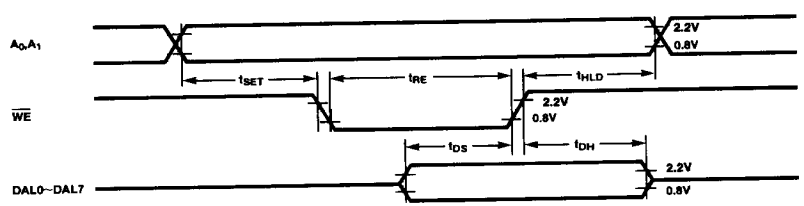
* These values are doubled when CLK = 4MHz.

Timing Diagrams

CPU Read Timing Diagram



CPU Write Timing Diagram



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Timing Diagrams
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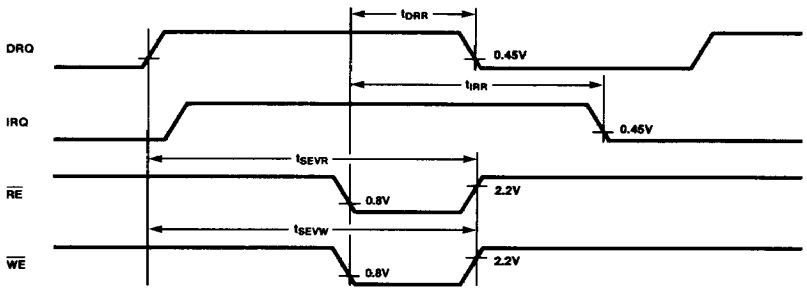
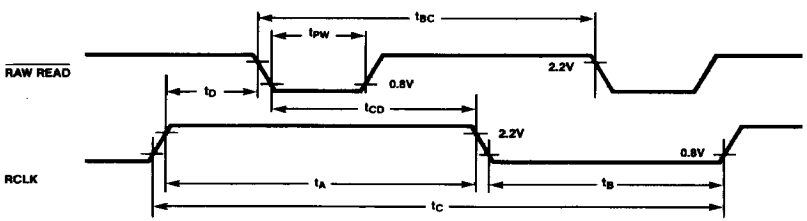
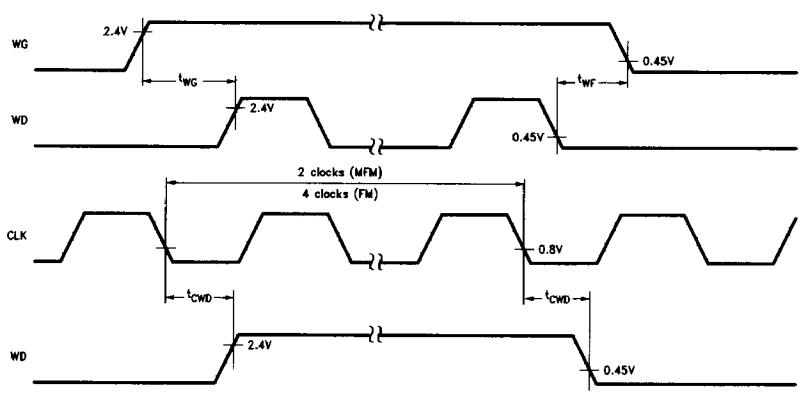
DRQ, IRQ Service and Release Timing Diagram



FDC Read Timing Diagram

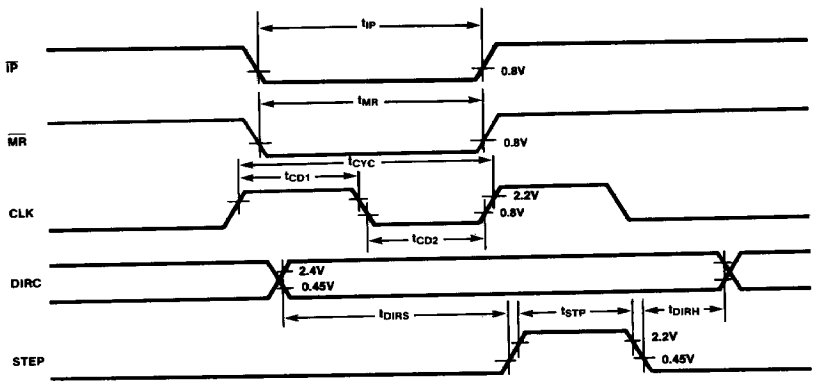


FDC Write Timing Diagram



Timing Diagrams
(Continued)

Other Timing Diagram



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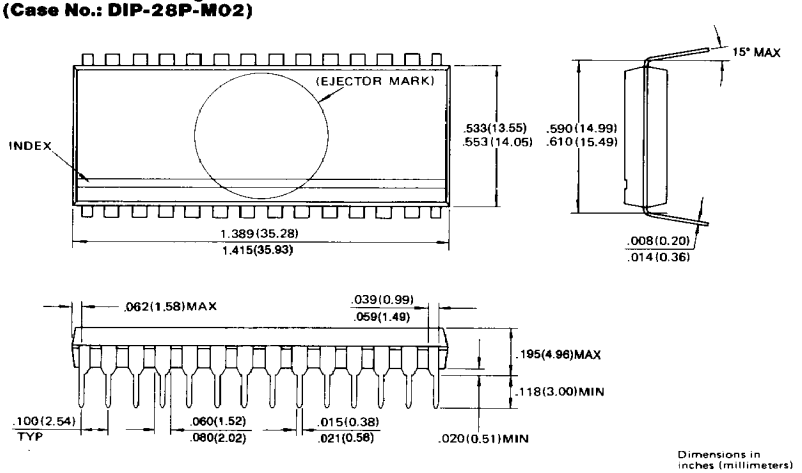
Package Dimensions
Dimensions in Inches
(millimeters)

28-Lead Plastic
Dual In-Line Package
(Case No.: DIP-28P-M02)



Dimensions in
inches (millimeters)